EE610

Analog/Digital VLSI Circuits

Project Report

Two-Stage Folded Cascode OTA Suitable for Large Capacitive Loads

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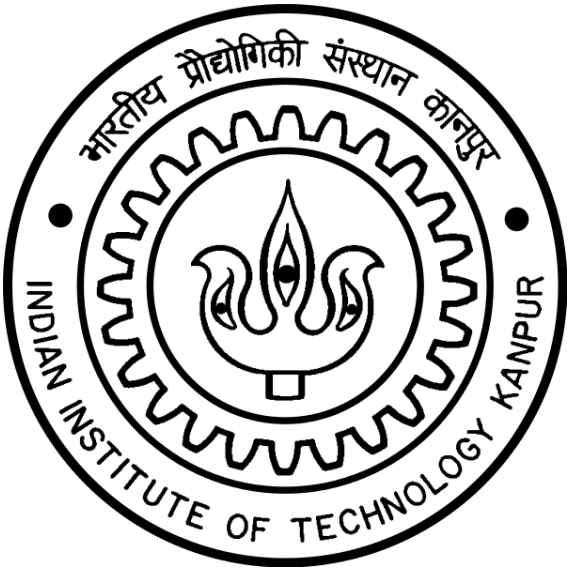


Abstract:

An enhanced single-stage folded cascode Operational Transconductance Amplifier (OTA) capable of driving large capacitive loads is mimicked. The design is optimized for low power, better output voltage swing, and slew rate. Circuits that adaptively bias the input differential pair and the current folding stage are employed. This provides class AB operation with dynamic current boosting and increased gain-bandwidth product (GBW). Results of the simulation of schematic and layout design, using Mentor Graphic Tool, in a 0.18 μm CMOS process is shown.

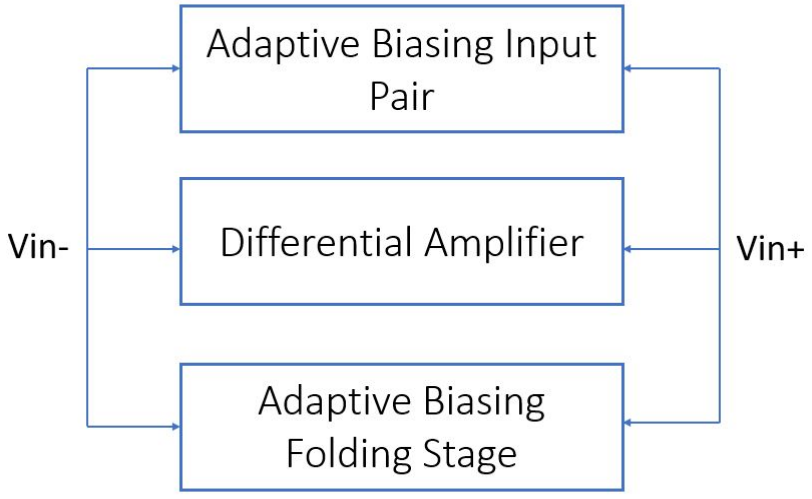
Introduction

Class AB amplifiers are widely employed in applications requiring low power consumption since they can yield large dynamic currents not limited by the quiescent currents. Hence low static power consumption can be achieved without degrading dynamic performance. These amplifiers usually employ an adaptive bias circuit for the differential pair to get the required current boosting. Such adaptive circuits can provide very low quiescent currents in order to have very low static power dissipation.

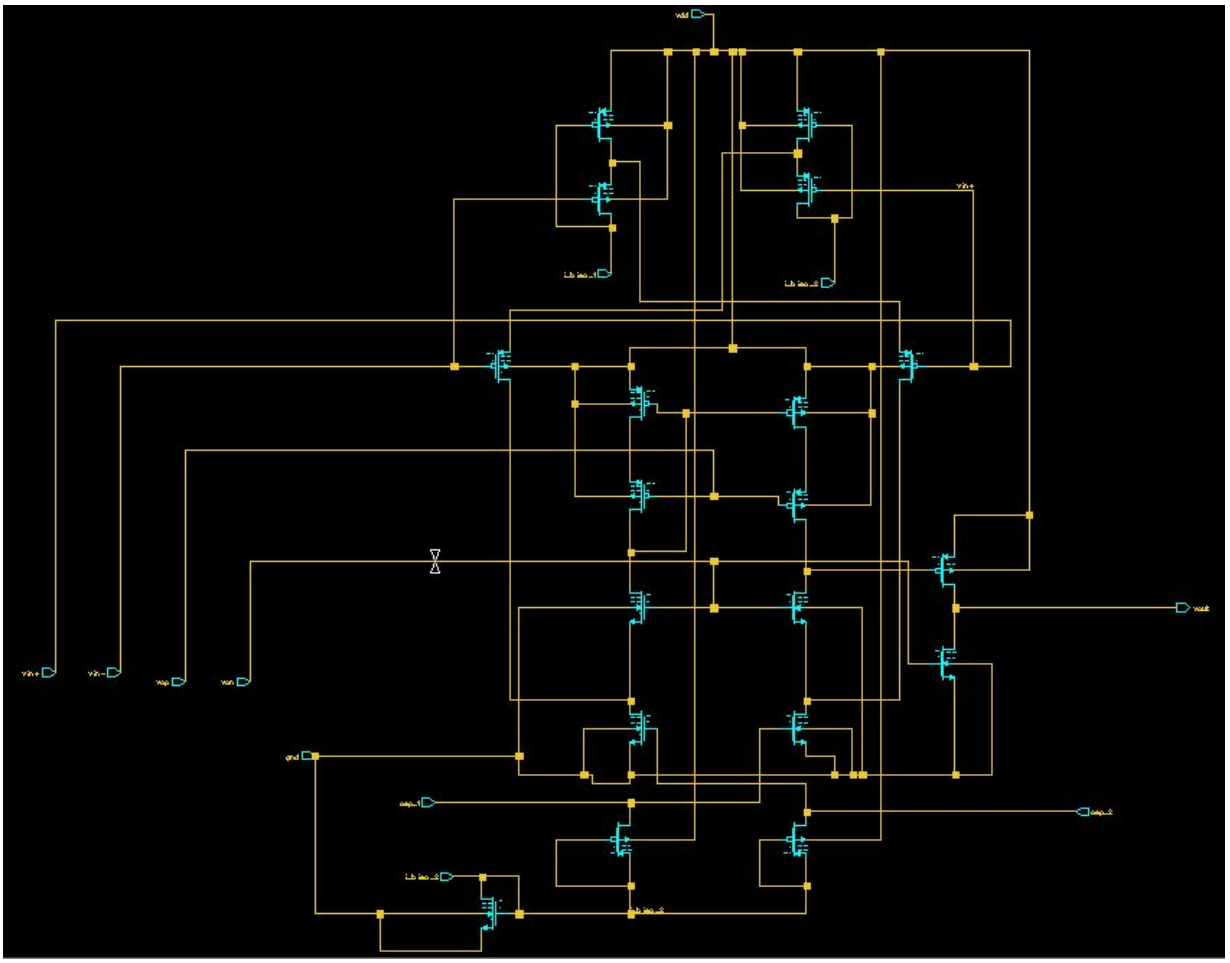
Several proposals have been reported to provide class AB operation to classic amplifier topologies like telescopic and current mirror OTAs. However, achieving class AB operation in a folded cascode amplifier is more complex. Adaptive biasing of the input pair is not effective by itself in this case since the bottom current sources at the folding stage limit the maximum output current. It is mandatory that the bias current sources also adapt to the input signal to achieve power efficiency.

A simple modification of the conventional folded cascode OTA is implemented here which enhances the performance of the amplifier with improved voltage swing.

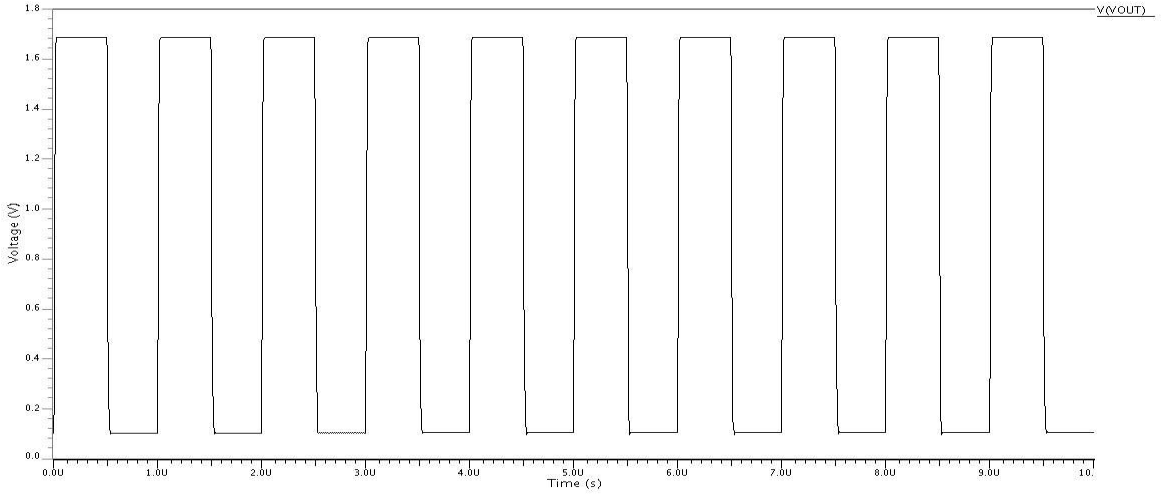
Idea - Circuit



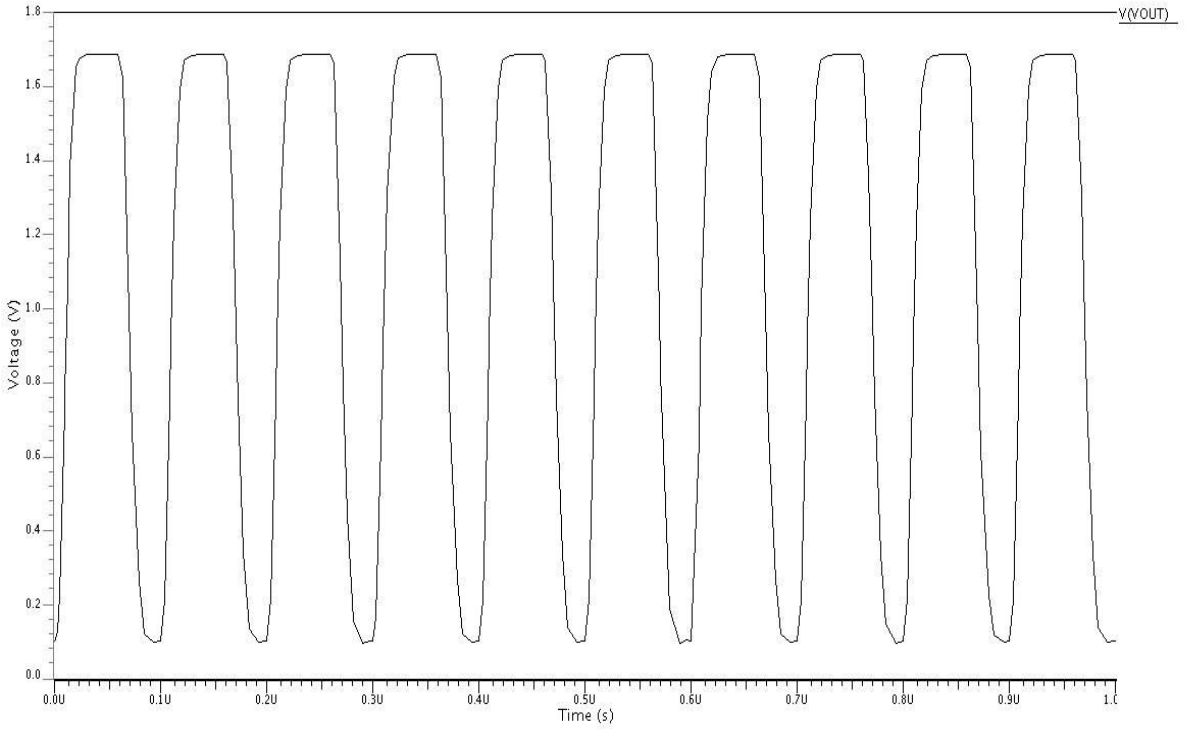
Schematic



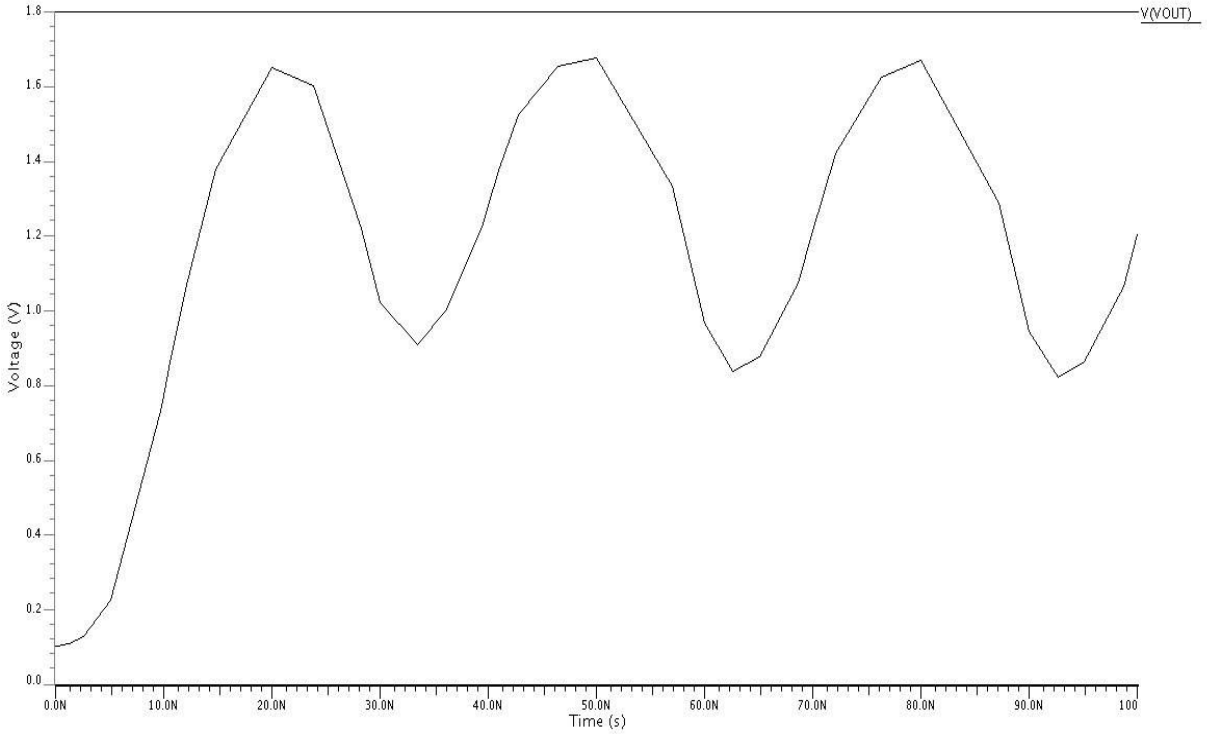
Simulation



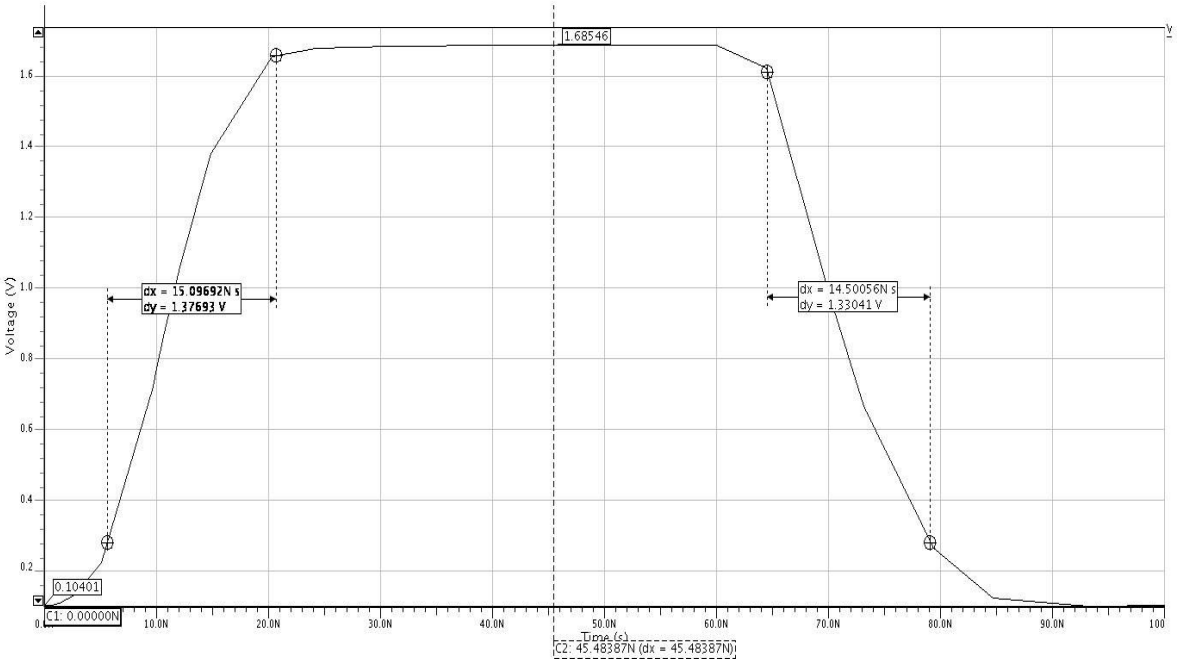
Corresponding to frequency - 1M



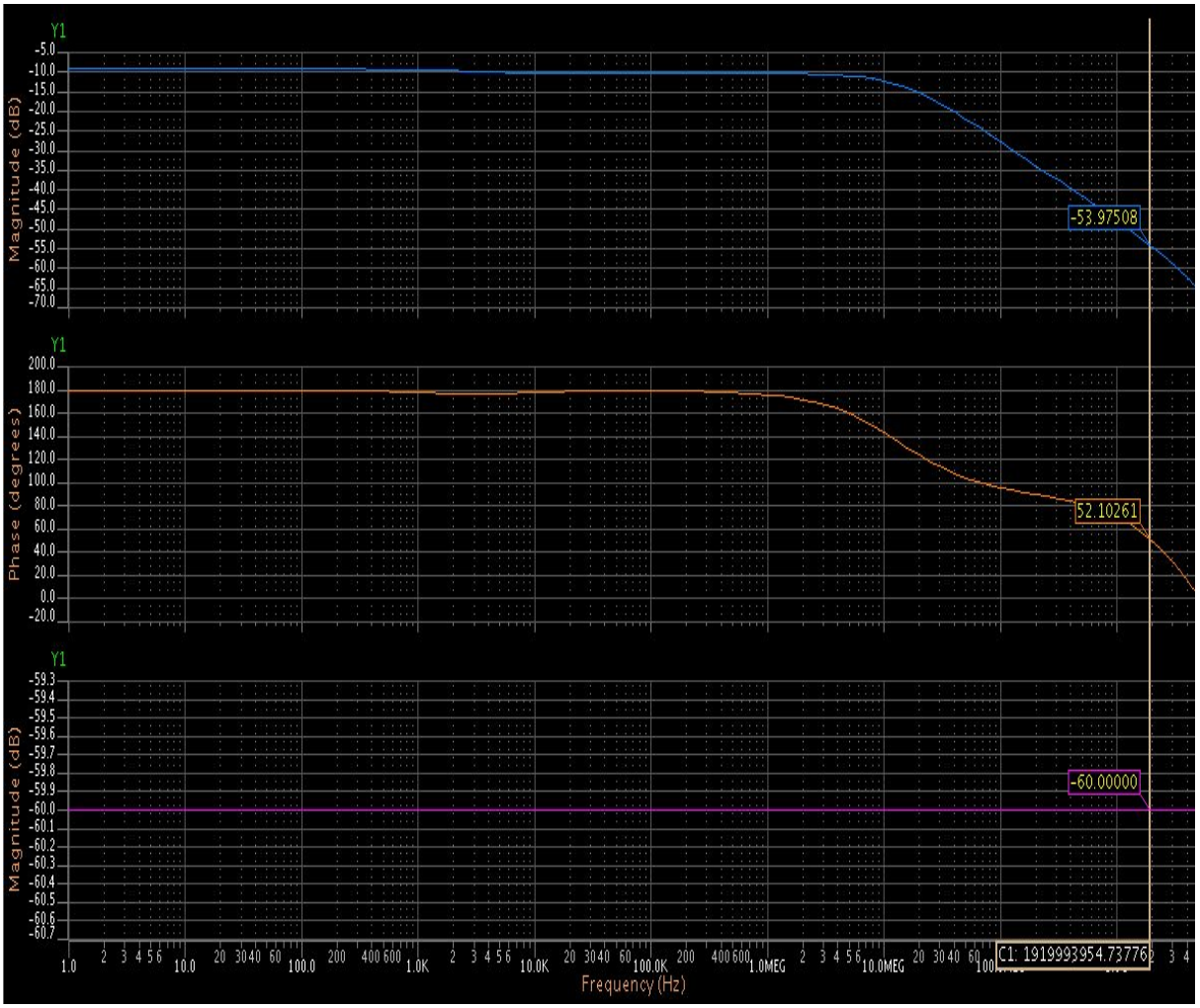
Corresponding to frequency - 10M



Corresponding to frequency - 50M

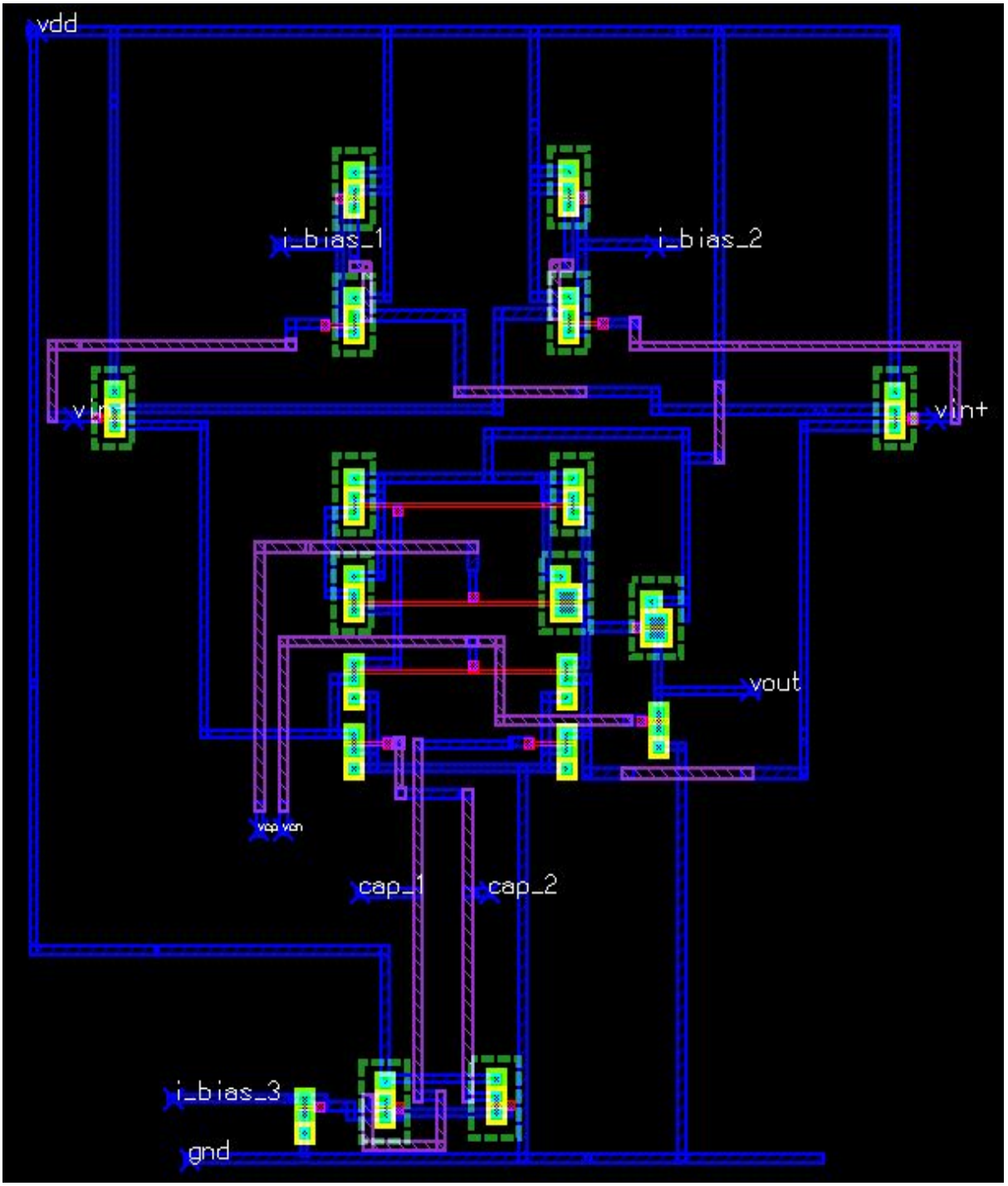


Slew Rate

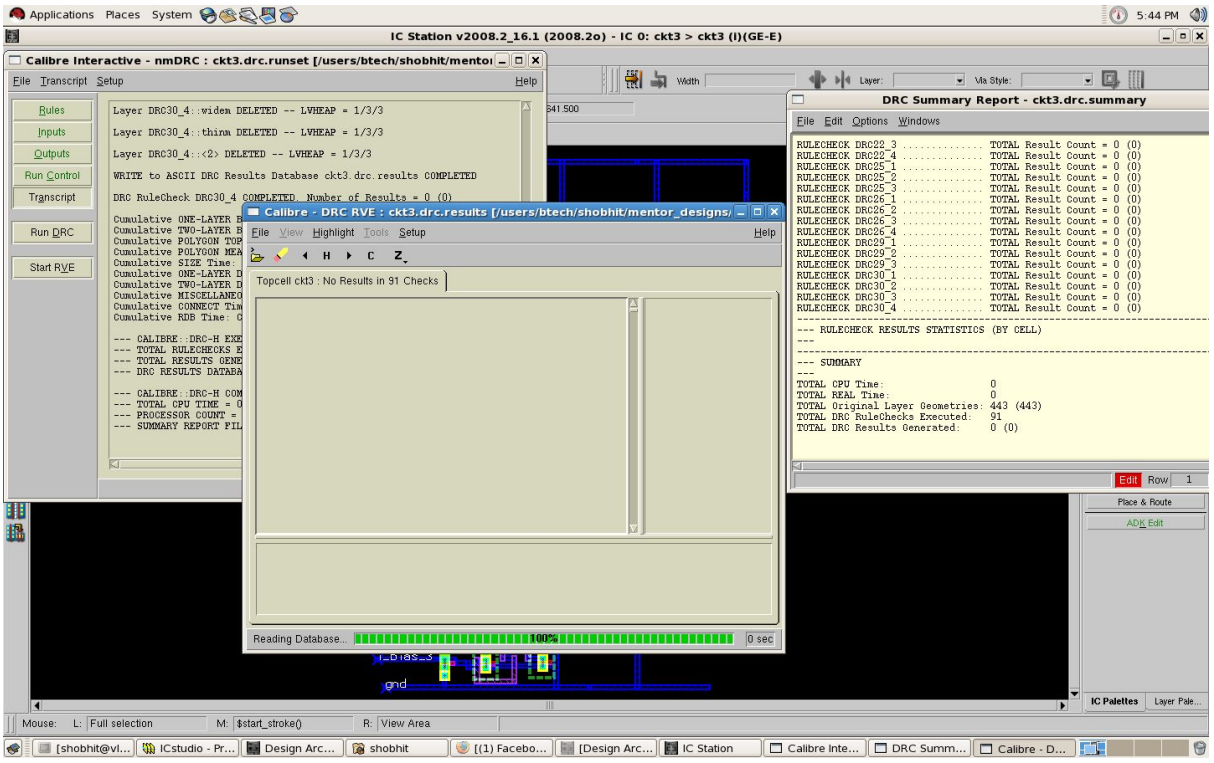


Bode Plot

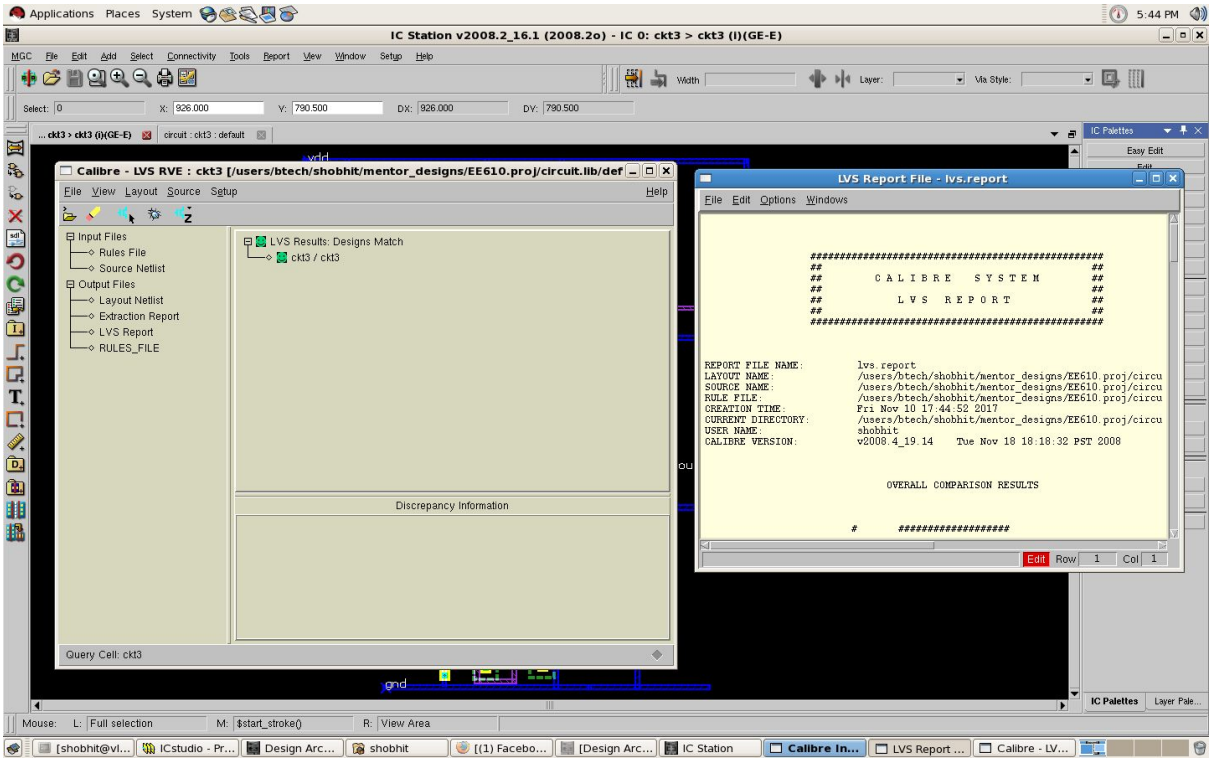
Layout



Checks

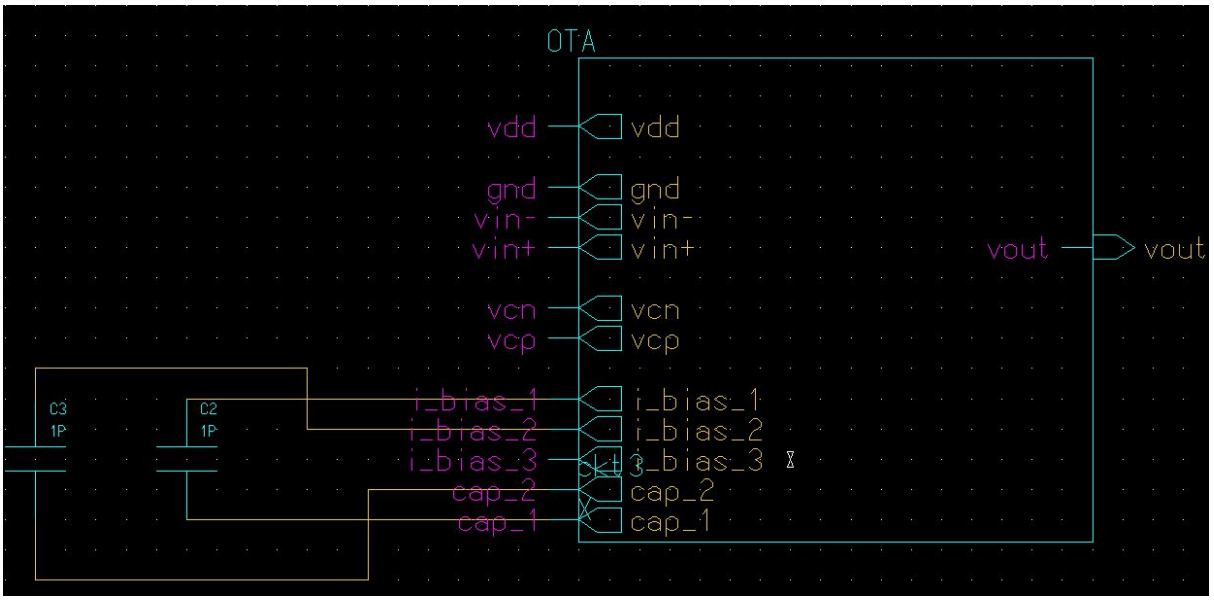


DRC Check ✓



LVS Check ✓

Symbol



Results

CMOS Process	180nm
Supply Voltage	1.8V
SR+	91.18 uV / usec
SR-	91.72 uV / usec
DC Gain	50db
PM	120°
Power	338.01uW
Area	0.0024 sq. mm.

Improvements

- Area optimized layout
- Power reduction by varying W/ L ratio

References

- Antonio Lopez-Martin, M. Pilar Garde & Jaime Ramirez-Angulo, “Enhanced Single-Stage Folded Cascode OTA Suitable for Large Capacitive Loads”, *IEEE Proceedings*, 2017