Verilog-A implementation and parameter extraction for BSIM4 like model

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***Abstract*—A threshold voltage based MOSFET model for terminal charge(s)/capacitance(s) and drain-to-source current, similar to BSIM4, is modelled using verilog-A. The model takes care of the second order effects such as mobility degradation with vertical field, velocity saturation, channel length modulation (CLM), and drain induced barrier lowering (DIBL). The I-V and C-V characteristics are plotted using Agilent IC-CAP simulation software. The parameters are extracted and tuned to fit the measured data. The model passed the for Gummel Symmetry Test for $V_{ds} \in$ (-600, 600) mV.**

I. Introduction

The report is majorly divided into two parts:

- Implementation of the threshold voltage based model to account for mobility degradation with vertical electric field, velocity saturation due to non-linear relation between electric field and velocity, CLM and DIBL effect.
- Parameter extraction and matching it to the measured data. The matched plots include sub threshold characteristics, I_{ds}-V_{gs} and g_m-V_{gs} in linear and saturation regions, and I_{ds}-V_{ds} and g_{ds}-V_{ds} for different gate and drain voltages.

II. Threshold voltage based model

The overall threshold voltage is modelled as

$$\begin{aligned} V_{th} &= VFB + \Phi_s + \gamma\sqrt{\Phi_s - V_{bs}} - K1.V_{bs} \\ &= VTH0 + \gamma(\sqrt{\Phi_s - V_{bs}} - \sqrt{\Phi_s}) - K1.V_{bs} \end{aligned}$$

where

$$\gamma = \frac{\sqrt{2q\epsilon_{si}N_{substrate}}}{C_{oxe}}$$

A. Mobility Degradation with vertical field

As a result of gate-body bias, a vertical electric field induces which confines charge carriers in the proximity of the gate oxide/substrate interface. Hence surface roughness scattering comes into the picture degrading the mobility. This degradation can be modelled as:

$$\mu_{eff} = \frac{U0.f(L_{eff})}{1 + \Big[UA\Big(\frac{V_{gsteff}+2V_{th}}{TOXE}\Big) + UB\Big(\frac{V_{gsteff}+2V_{th}}{TOXE}\Big)^2\Big] \times \Big(1 + UC.V_{bseff}\Big) + UD\Big(\frac{V_{th}.TOXE}{V_{gsteff} + 2\sqrt{V_{th}^2 + 0.0001}}\Big)^2}$$

$$f(L_{eff}) = 1 - UP.exp\Big(-\frac{L_{eff}}{LP}\Big)$$

$U0$ is the intrinsic mobility of the device. UA, UB, UC, UD and UP are the parameters. V_{th} is the threshold voltage and V_{gsteff} is the effective gate source voltage. $TOXE$ is the electrical gate equivalent oxide thickness and L_{eff} is adjusted length of the device.

B. Velocity Saturation

For higher drain voltages, the lateral electric field increases and results in increased lattice interactions. This leads to reduced mobility, which is modelled as:

$$\mu \propto \frac{1}{1 + \frac{V_{ds}}{L.E_{sat}}}$$

$$\implies I_{ds} \propto \frac{1}{1 + \frac{V_{ds}}{E_{sat}.L}}$$

$$E_{sat} = \frac{2.VSAT}{\mu_{eff}}$$

Here E_{sat} represents the value of electric field at which the velocity of majority carriers reaches saturation (V_{sat}).

C. Channel Length Modulation

In this second order effect, the I_{DS} - V_{DS} curves show a dependence on V_{DS} which is modelled as:

$$I_{ds} \propto (1 + \lambda.V_{ds})$$

where λ is a parameter.

D. Drain Induced Barrier Lowering

Higher drain voltage results in lowering of the potential barrier i.e threshold voltage. This effect is pronounced in short channel devices and is known as DBIL effect.

It is modelled as a change in V_{th} as follows:

$$\Delta V_{th,DIBL} = -\theta_{th,DIBL}.(ETA0 + ETAB.V_{bs}).V_{ds}$$

$$\theta_{th,DIBL} = \frac{0.5}{cosh\Big(\frac{DSUB.L_{eff}}{lt}\Big) - 1}$$

$$lt = \sqrt{\frac{\epsilon_{Si} t_{ox} X_{dep0}}{\epsilon_{rox}}}$$

$$X_{dep0} = \sqrt{\frac{2\epsilon_{Si}\phi_s}{q.NDEP}}$$

Drain Current

Single equation for drain source current in all operating regions is given by:

$$I_{ds} = \frac{\mu_{eff}.K.V_{gsteff}.\left(1 - \frac{m}{2}\frac{V_{dseff}}{V_{gsteff}+2v_t}\right)\times}{1 + \frac{V_{ds}}{L.E_{sat}}} \\ V_{dseff}.(1 + \lambda.V_{ds})$$

$$V_{gsteff} = \frac{2n.v_t \ln\left(1 + \exp\frac{V_{gs}-V_{th}}{2n.v_t}\right)}{1 + 2n.\exp\left(-\frac{V_{gs}-V_{th}-2V_{off}}{2n.v_t}\right)}$$

Terminal Charge Model

The approach taken to model the terminal charges is follows:

$$\alpha = 1 - \frac{V_{dseff}}{V_{dsat}}$$

Inversion charge is given by

$$Q_{inv} = -\frac{2}{3}.W.L.C_{ox}.V_{gsteff}.\frac{1 + \alpha + \alpha^2}{1 + \alpha}$$

Considering 40/60 partitioning scheme,

$$Q_d = -\frac{2}{15}.W.L.C_{ox}.V_{gsteff}.\frac{3\alpha^3 + 6\alpha^2 + 4\alpha + 2}{(1 + \alpha)^2}$$

$$Q_s = -\frac{2}{15}.W.L.C_{ox}.V_{gsteff}.\frac{2\alpha^3 + 4\alpha^2 + 6\alpha + 3}{(1 + \alpha)^2}$$

Bulk charge is given by

$$Q_B = -W.L.C_{ox}.(m-1)\times \\ \left[\frac{V_{gsteff}}{m}\left(1 - \frac{2}{3}\frac{1 + \alpha + \alpha^2}{1 + \alpha}\right) + 2.(2\phi_s - V_{bs})\right]$$

Accumulation charge is given my

$$Q_{acc} = W.L.C_{ox}.(V_{bs} - VFBCV)$$

Smoothing of $(V_{bs} - VFBCV)$ is done to correct the gate charges in accumulation region. For doing this maximum function and a parameter $D4$ is used.

III. Parameter Extraction and Curve Fitting

Simulation is performed for MOSFET with length 0.8μm and width 1μm. We extracted:

- $NSUB$, VFB, N, $VOFF$ from linear region (log scale) in $I_D V_G$ curves.
- $U0$, UA, UB, UC, UD, UP, and LP from linear region (linear scale) in $I_D V_G$ curves.
- $ETA0$, $ETAB$, $DSUB$, $VSAT$ from saturation region in $I_D V_G$ curves.
- $LAMBDA$, $DELTA$ from $I_D V_D$ curves.

Rest current parameters were tuned collectively. $K1$ parameter is introduced to tackle the V_{BS} dependent spacing between the curves. CG, CD and CB are the overlap capacitance parameters accounting for the overlap between gate-source, gate-body and gate-drain regions.

Different parameters extracted by fitting data points are as follows:

Note: all values are in SI units

TABLE I
PARAMETERS USED FOR THE FOLLOWING PLOTS

Model Parameters	Extracted Value
L	800.0n
W	1.0u
TOXE	3.109n
VFBCV	-838.2m
VOFF	-229.1m
VOFFCV	44.56u
EOT	1.400n
DSUB	560.0m
ETA0	80.00m
ETAB	700.0m
NSUB	8.465E+23
DELTA	17.82m
VSAT	90.86K
K1	-13.84m
U0	29.63m
UA	719.6p
UB	3.338E-19
UC	-23.82m
UD	0.000
UP	0.000
LP	12.41n
LAMBDA	57.28m
D4	61.11m
M	1.037
N	1.522
NCV	2.066
MCV	2.183
UCV	151.0m
XX	2.070
VFB	-864.6m
CG	19.81f
CB	1.205f
CD	1.585E-25

Simulation Results

Figure 1 presents the TCAD data fitted current voltage characteristics namely: I_DV_G and I_DV_D characteristics. I_DV_G curves are plotted with $V_{DS} = 50mV$ and $V_{DS} = 1V$ with V_{BS} varying from 0V to -2V. For $V_{GS} = 50mV$ curves are plotted for both linear and log scale. I_DV_D curves are plotted for V_{GS} varying from 0.4V to 2V. Transconductance g_m for both linear and saturation regions, and output conductance g_{ds} are also plotted for the same bias conditions as above.

Figure 3 presents TCAD data fitted C_{GG}, C_{GS}, C_{GD} and C_{GB} for V_G varying from -2V to 2V and $V_{DS} = 0V$.

Figure 4 presents C_{GG}, C_{GS}, C_{GD} and C_{GB} for V_{DS} varying from 0V to 2V for three different values of V_{GS} i.e. for $V_{GS} = 1V, 1.5V, 2V$.

To ensure nice fit new parameters such as XX (for inversion region capacitance used in $V_{GSteff,CV}$), UCV (for correction in $V_{DSat,CV}$ due to velocity saturation effect) and $D4$ (for smoothing of $V_{GB} - VFBCV$ to get smooth accumulation charge, and hence smooth gate charge) are introduced. Bad fitting of Cvs.V_{DS} curves is due to the introduction of the XX parameter unwisely.

A. Gummel Symmetry Test

Gummel symmetry test was performed on the model to check its performance for both positive and negative bias (V_{ds}). On IC-CAP the gummel test worked for voltages upto $600mV$ as shown in Figure 5. On Hspice full the model seemed to work for +/- 100V.

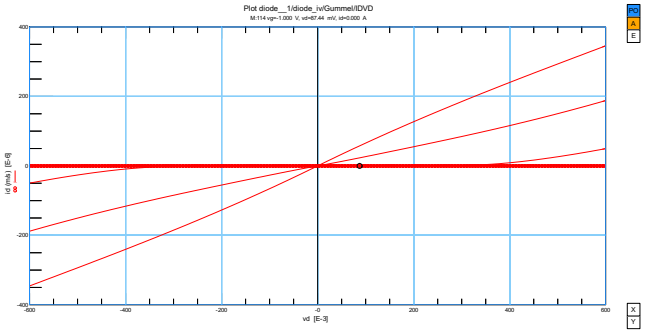

Fig. 5. Gummel Symmetry Test $V_{ds} \in$ (-600,600) mV

B. Derivative Test

$g_{m,lin}$, $g_{m,sat}$ and g_{ds} are continuous till third derivative. The results are shown in the Figure 2. Over model work for $V_{ds} < 0$ as well.

C. Inverter Characteristics

To test our model for inverter characteristics, we created a netlist for pseudo-NMOS inverter and simulated the same on Hspice. The model functioned properly and the simulation converged. Figure 6 shows its corresponding I-V characteristics.

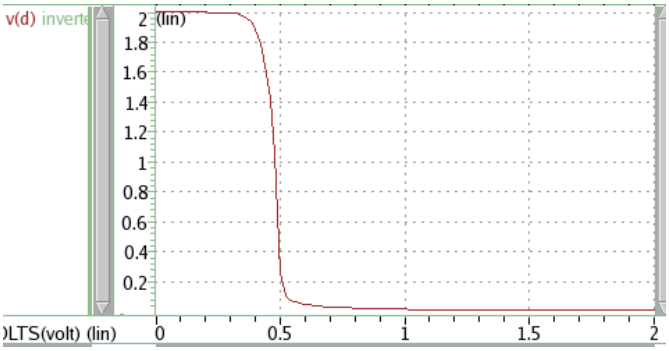

Fig. 6. Pseudo-NMOS I-V characteristics.

D. Issues encountered during parameter extraction

While working on IC-CAP simulator, we faced a lot of issues.

- Major issue was unfamiliarity with the tools. We acquainted ourselves with the tools by the means of demos and manuals.
- For some simulations HSPICE/Spectre worked fine but ADS gave DC convergence issue, it was due to some out of order default values of some parameters.
- Modelling of the gate charge when we move across the depletion region was an issue as it was an implicit equation. A smoothing function involving V_{GB} and $VFBCV$ was used. A maximum function was used to smooth $V_{GB} - VFBCV$ to zero for the values of V_{GB} larger than $VFBCV$.
- While modeling the capacitance we had to modify the effective V_{GSt} by introducing a parameter XX which determines the capacitance in the strong inversion region. We also introduced another parameter UCV to fit the curve by accounting for velocity saturation effect.
- Initially, the current model was not working for $V_{ds} < 0$. So, the source-drain terminals were reversed and thus the current also became negative.

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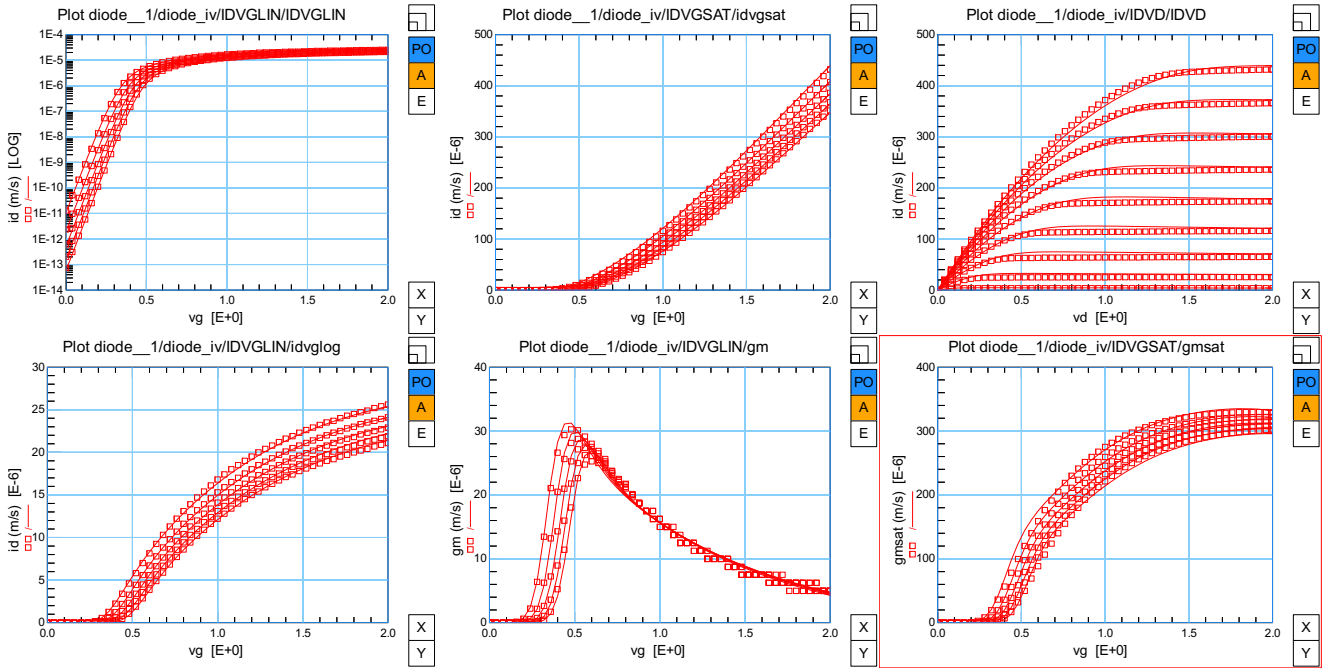

Fig. 1. (Left-Top) I_{ds} vs V_{gs} curve (log scale) in linear region; (Left-Bot) I_{ds} vs V_{gs} curve in linear region; (Mid-Top) I_{ds} vs V_{gs} curve in saturation region; (Mid-Bot) g_m vs V_{gs} curve in linear region; (Right-Top) I_{ds} vs V_{ds} curve; (Right-Bot) $g_{m,sat}$ vs V_{gs} curve;

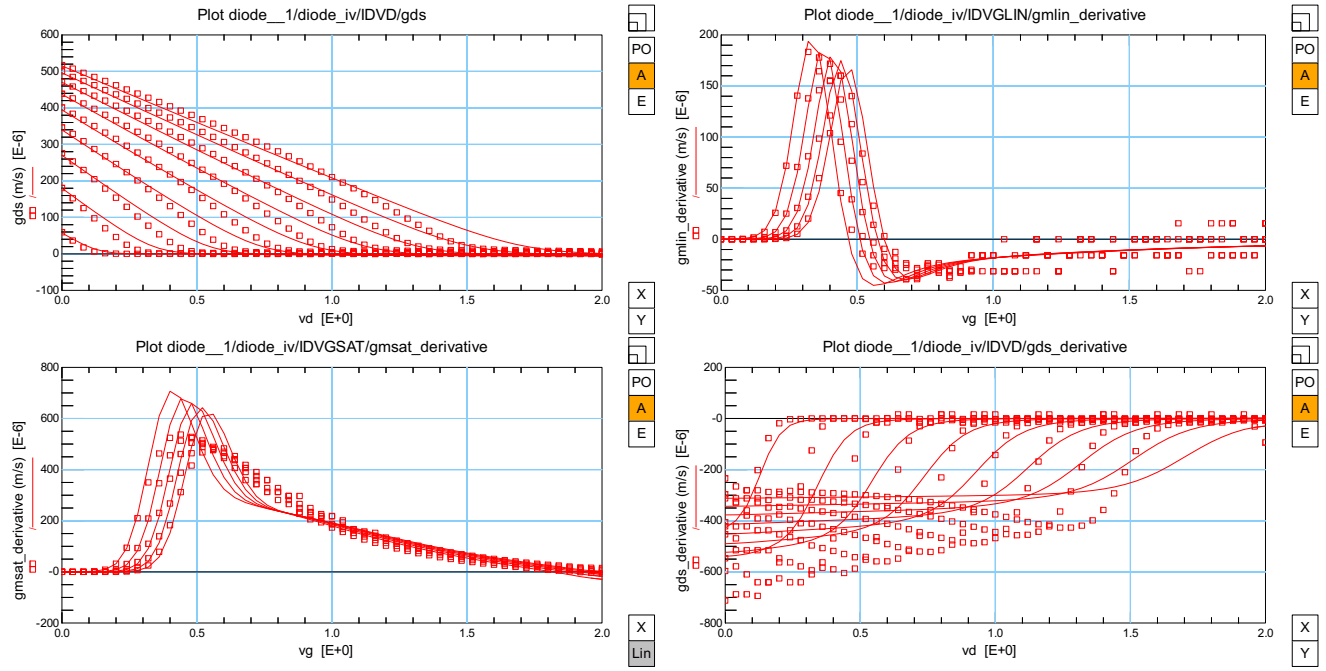

Fig. 2. (Left-Top) g_{ds} vs V_{ds} curve; (Left-Bot) $derivative(g_{m,sat})$ vs V_{gs} curve in saturation region; (Right-Top) $derivative(g_{m,lin})$ vs V_{gs} curve in linear region; (Right-Bot) $derivative(g_{ds})$ vs V_{ds} curve;

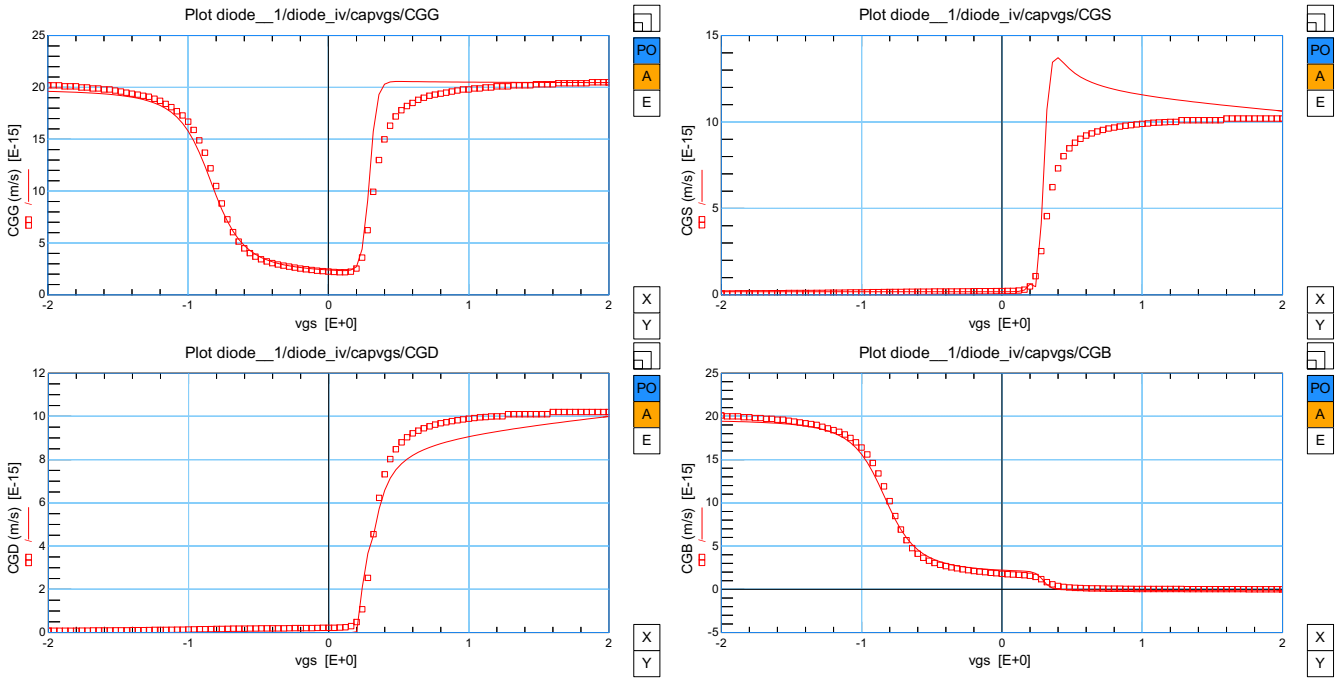

Fig. 3. (Left-Top) C_{gg} vs V_{gs} curve; (Left-Bot) C_{gd} vs V_{gs} curve; (Right-Top) C_{gs} vs V_{gs} curve; (Right-Bot) C_{gb} vs V_{gs} curve;

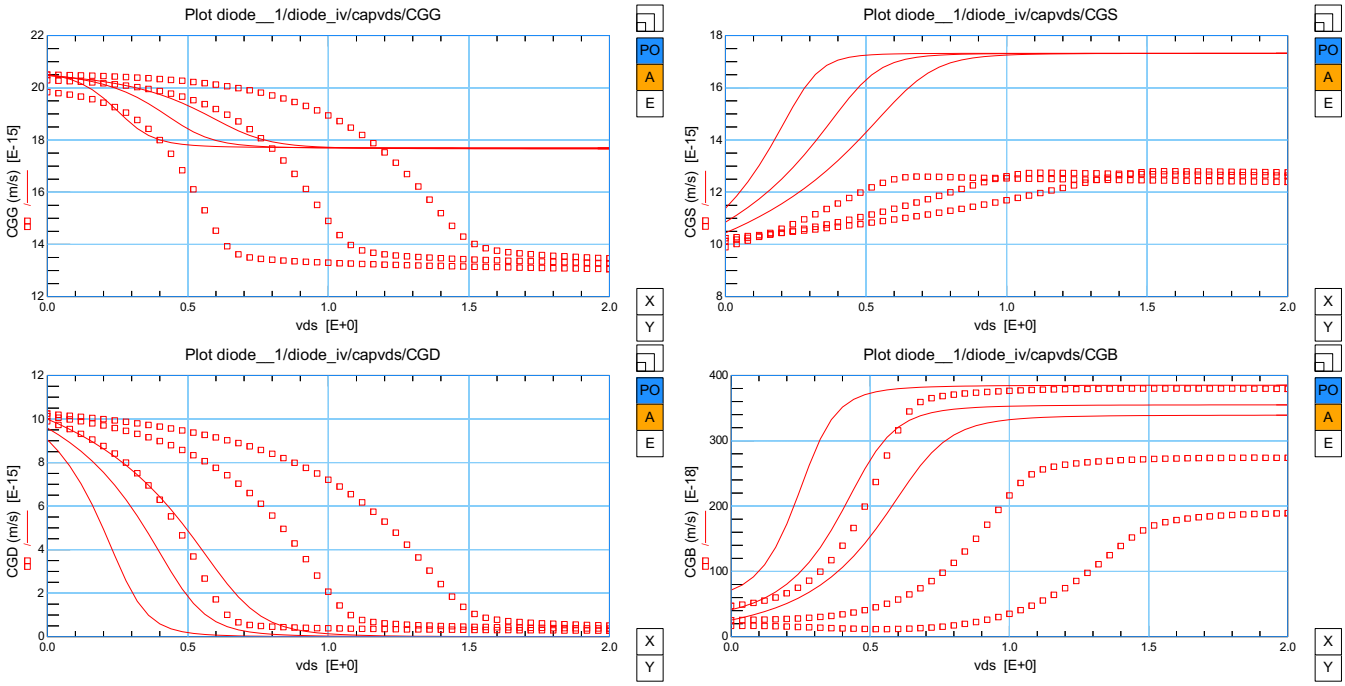

Fig. 4. (Left-Top) C_{gg} vs V_{ds} curve; (Left-Bot) C_{gd} vs V_{ds} curve; (Right-Top) C_{gs} vs V_{ds} curve; (Right-Bot) C_{gb} vs V_{ds} curve;