Binary Metal-oxide RRAM at a glimpse

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***Abstract*— This document briefly states the journey of binary metal-oxide resistive switching random access memory (RRAM). It encompasses the switching mechanism, design and electrical characteristics of various binary metal-oxide RRAM. It also brings to light the use of RRAM for non-volatile memory application and neuromorphic computing. The recent advancements to solve issues of uniformity, endurance, multi-bit operation and scaling are also discussed.**[1]

I. INTRODUCTION

Some of the early reports that showed the unique property of oxides, i.e being capable of abruptly switching from insulator state into a conductive state, were [1]-[3]. The device structure consisted of a thin oxide layer sandwiched between two metal electrodes, also known as metal-insulator-metal (MIM) structure. The device switched between two resistive states: high-resistance state (HRS) and low-resistance state (LRS). Since the research was still premature it couldn't be directly implemented for memory applications. The interest in this field rekindled in during the late 1990s when resistive switching was showed in various complex metal oxides ($SrTiO_3$ [4], $SrZrO_3$ [5]), followed by binary metal oxides (NiO [6] and TiO_2 [7]). A major breakthrough occurred when Samsung presented [8] at IEDM that demonstrated that OxRRAM (an alias for metal-oxide RRAM) is highly compatible with conventional CMOS technology by fabricating one-transistor-one-resistor (1T1R) OxRRAM memory cells. They also discussed cell and device properties such as endurance cycles, programming speed and data retention time. In light of this, metal-oxide RRAM is expected to revolutionize memory technology by its low cost, nonvolatile memory with programming speed in tens of nanosecond, over 10^6 endurance cycles, and potentially low power/energy consumption.

Numerous researches are performed in order to understand and exploit resistive switching mechanisms. It has been showed that the switching behavior not only depends on the oxide material but also on the choice of metal electrodes and their interfacial properties. This document is structured to present resistive switching mechanism in Section-II, RRAM memory arrays in Section-III, key performance metrics in Section-IV, and finally future outlook in Section-V. The scope of this document is limited to selected binary metal oxides (HfO_x, AlO_x, NiO_x, TiO_x, and TaO_x; where x represents the oxide composition of respective non-stoichiometric compounds).

II. RESISTIVE SWITCHING MECHANISM

Few important terminologies:

- Set process: Switching from HRS to LRS.
- Reset process: Switching from LRS to HRS.
- Electroforming or Forming process: The process of increasing voltage over set voltage in order to trigger switching behavior; usually required for fresh samples (in its initial resistance state).
- Switching modes:
  - Unipolar: Switching direction depends only on the amplitude of the applied voltage, not its polarity, i.e. set and reset can occur at same polarity.
  - Bipolar: Switching direction depends on the polarity of the applied voltage. If set occurs at one polarity, reset will only occur at reverse polarity.

  Independent of the switching mode, in order to prevent permanent breakdown of the dielectric, set compliance is enforced by the memory cell selection transistor/diode or a series resistor.

To understand why a simple I-V curve fitting may be insufficient to represent conduction of metal-oxide RRAM lets have a look at various possible paths that an electron can take to pass from cathode to anode [9]:

- Schottky emission: thermally activated electrons injected over the barrier into the conduction band.
- Fowler-Nordheim (F-N) tunneling: electrons tunnel from the cathode into the conduction band; usually occurs at high field.
- Direct tunneling: electron tunnel from cathode to anode directly; usually occurs when the oxide is thin enough.
- For oxide containing substantial number of traps (e.g., oxygen vacancies), trap-assisted tunneling contributes to additional conduction, including the following steps:
  - tunneling from cathode to traps
  - emission from trap to conduction band (Poole-Frenkel emission)
  - F-N-like tunneling from trap to conduction band
  - trap to trap hopping or tunneling
    - Mott hopping when the electrons are in the localized states
    - metallic conduction when the electrons are in the extended states depending on the overlap of the electron wave function
  - tunneling from traps to anode

Dominant conduction mechanism for a particular metal-oxide RRAM among the aforementioned processes depends on its dielectric properties (bandgap or trap energy level, etc.), fabrication process conditions (annealing temperature, annealing ambient, etc.), and properties of oxide-electrode interfaces (interfacial barrier height).

[1]Flow of the document and study is adapted from [26]

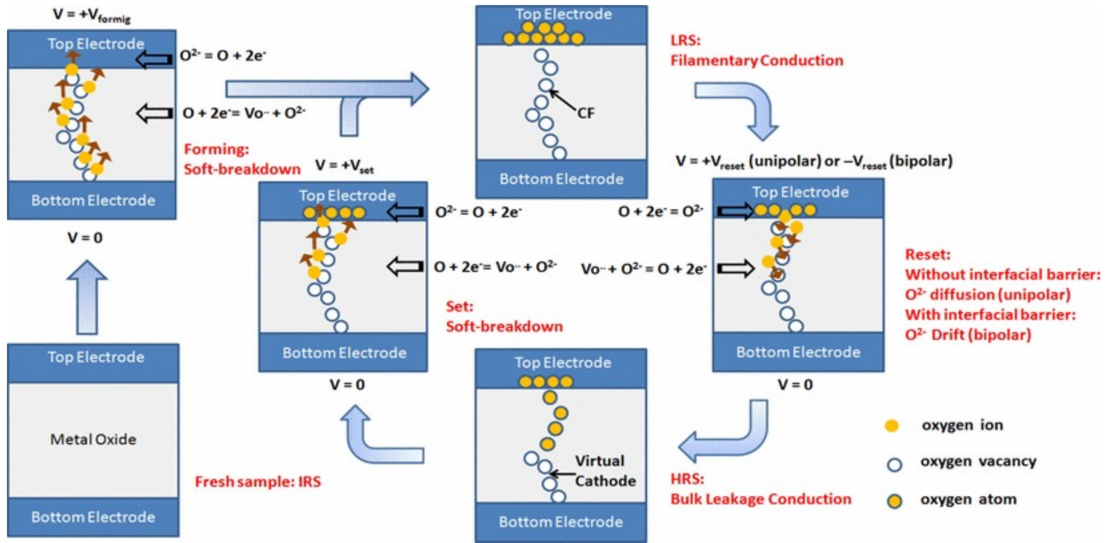

Fig. 1. Schematic illustration of the switching process in the simple binary metal-oxide RRAM. Adapted from [21].

For a given configuration of the conductive filaments (CFs), at the low bias regime the I-V characteristics are mainly determined by the electron conduction process, while at the high bias regime the motion of oxygen ions/vacancies would distort the configuration of CFs and thus change the current. Determining a detailed picture on the physical mechanism of resistive switching for metal-oxide RRAM is still an active area of research.

A. Forming/Set

The forming process is depicted as soft breakdown of the dielectric [10]. This process is not abrupt, rather it is exponentially dependent on time [11]. On application of high electric field across the oxide layer, some oxygen atoms get knocked out of the lattice and are collected in the anode. Simultaneously, defects in the bulk oxide are generated. The left deficiencies of oxygen atoms (vacancies) form several conduction paths which are known as conduction filaments [12]. This path can also be formed by metal precipitates [13].

Since a fresh sample has fewer defects, the initial resistance of the sample is larger than that in HRS during the following switching cycles, and hence the forming voltage is greater than the set voltage. This is the case because not all vacancies of oxygen are recovered in the reset process. The remaining defect-rich region is also known as the ”virtual electrode.”

It is not ideal to have a lager forming voltage. Therefore a considerable amount of research is done in order to achieve the so-called ”forming-free” device. It is observed that the forming voltage decreases linearly with a decrease in oxide thickness [14]-[16]. It was also found that forming strongly depends on film deposition conditions [17].

B. Unipolar/Bipolar Reset

Existing reset mechanism models are incapable to explain the all experimental observations for both switching modes. For eg., it appears that the thermal dissolution model [18] is capable of explaining parts of unipolar switching characteristics (NiO_x), while the ionic migration model [19] is capable of explaining parts of bipolar switching characteristics.

It was discovered that switching mode is not solely the property of the oxide material but it also depends on the properties of the oxide-electrode interface. Acknowledging the fact that oxygen ion migration is responsible for reset mechanism, in the year 2010 Yu et al. [20] proposed a phenomenological model providing a unified explanation for both the unipolar and bipolar resistive switching mechanisms. Fig.1 presents the schematic illustration of the switching processes. Soft breakdown of dielectric happens during the forming process and the oxygen ions drift towards the anode. Sometimes the anode material reacts with oxygen to form oxide-electrode interface. Thus, this anode/oxide-electrode behaves as an “oxygen reservoir” [22]. In the LRS, the current flows through the CFs formed. During the reset process, oxygen ions migrate back to partially compensate the oxygen vacancies. This is how the memory cell returns back to the HRS. For the unipolar switching mode, the Joule heating effect activates and aids the diffusion of oxygen ions to attain proximity to CFs [23]. Thus it relatively takes a larger value of reset current to increase the temperature around CFs. On the other hand, for bipolar switching mode, the thermal diffusion is not sufficient and thus requires a negative electric field to assist the oxygen ion movement. A few alternate theories/models were proposed in [24] and [25].

III. RRAM Memory Arrays

A. Cell Design

Knowing that the forming/set current is relatively larger than the operating current, we need to limit the maximum current in order to preserve the memory device [14] and [27]. High resistance and fast response time make the transistor an attractive element to clamp the maximum current. But one

must watch for high parasitic capacitance while integrating transistor and RRAM into a 1T1R device. A high capacitance could cause an overshoot in current which in turn would increase reset current [14]. [28] presents contact RRAM in which the RRAM is realized in a small contact hole directly on the MOSFET's source/drain contact. This method minimizes the parasitic capacitance and clamps the reset current around 150μA.

B. Process Technology

There isn't "one" golden material for metal-oxide RRAM formation. But during fabrication one must take care that the fabrication process doesn't damage the oxide layers. We have gone through the advantages of forming-free devices. These are generally achieved by decreasing the thickness of the oxide layer. However, this may result in an increase in initial defect density and severe decrease in the resistance corresponding HRS. The breakdown voltage of the dielectric depends on the defect count rather than the defect density. Further, it was observed that there is a linear relationship between the size of the device and its breakdown voltage [29].

C. Memory Array

With a 1T1R memory cell, NOR-type memory array is preferred to effectively clamp the forming/set current. 3-D stacking of RRAM in a cross-point architecture is also contemplated.

IV. KEY DEVICE PERFORMANCE METRICS

A. Uniformity

Uniformity is a major barrier to large scale production of metal-oxide RRAM devices. The uniformity problem exists in two forms: Temporal (cycle to cycle) and Spatial (device to device). The variation is present in the parameters like resistances in LRS and HRS as well as switching voltage. It is understood that the LRS resistance variation is caused because of difference in sizes of CFs. This can be mitigated by narrowing the switching area which in turn would reduce the number of filament paths. HRS resistance variation is attributed to variation in ruptured CFs' length. Since there is an exponential dependence of tunneling current on tunneling length, a small variation in tunneling length would be magnified. Therefore variation in HRS is a more critical problem.

In order to solve the problem of uniformity, significant efforts have been made. Some of the methods are as follows:

- Engineering the electrode/oxide interface by embedding appropriate buffer layers. For eg., in [30], Yu et al. proposed to insert a layer of Al between TiN electrode and HfO_x bulk oxide.
- Inserting the seeds in the bulk oxide to confine the CFs paths using the local electric field enhancement effect. For eg., Liu et al. [31] proposed to implant Ti atoms into ZrO_x memory.
- Confining the path of CFs by redesigning the cell structure or reducing the cell area. For eq., in [32], the NiO layer was placed on the sidewall between the top electrode and the bottom electrode in a cross-point architecture. This enhanced the electric field at the bottom corner of the top electrode and thus device uniformity improved.
- Programming methods:
  - Ramping the reset voltage. In this way HRS can be increased to even higher values. However, in order to constraint the LRS higher set voltage should be applied such that stronger CFs are formed.
  - Cycle to cycle uniformity can also be improved by using a series of pulses instead of a single pulse [33] or multiple ramped pulses [34].

B. Endurance

Operating metal-oxide RRAM from cycle to cycle tends to reduce HRS which can finally get struck in LRS during the device failure. This can be caused by the accumulation of oxygen vacancies at/near the oxide-electrode interface, CFs or the oxide matrix. Sometimes it is also observed that during the worn phase of LRS, it tends to increase. This may be caused by the formation of an interfacial layer between the oxide and the electrode [35]. The problem of oxygen vacancy accumulation can be resolved by a verified reset operation [36] which assures of putting the oxygen back to the switching region. But this method shouldn't be overused as over-reset CFs are difficult to set [35]. The nonuniform distribution of oxygen vacancy can also be aggravated from the nonuniform electric field which may arise from the rough bottom electrode.

C. Retention

A non-volatile memory is expected to retain data for longer than ten years in a temperature around 85°C (operating temperature) with a constant series of read pulses (electrical stress). But this should not come at the cost of programming speed ($\sim$10ns).

D. Multi-bit operation

For high-density memory applications, having more than one bits of digital data per set is very desirable. Most of the RRAM oxide materials were reported to be capable of multilevel cell (MLC) operation. The largest number of resistance levels reported were five levels without verification for HfO_x [14] and eight levels with verification for WO_x [37]. A few important points regarding the MLC operation:

- Enough resistance window between any two states.
- Uniformity of each state.
- Cycling endurance for each state.
- Thermal stability of data in each state.
- Immunity to Read pulses for each state.

E. Scalability

A major motivation towards metal-oxide RRAMs was its scalability to the nanometer regime. In the year 2011 [38], HfO_x memory device was scaled down to 10nm X 10 nm and was able to retain good performance.

	NiO IEDM 2004	Cu_xO IEDM 2005	Ti:NiO IEDM 2007	TaO_x IEDM 2008	Ti/HfO_x IEDM 2008	Ti/HfO_x IEDM 2009 &2010	WO_x IEDM 2010	ZrO_x/HfO_x IEDM 2010	N:AlO_x VLSI 2011	TaO_x/Ta_2O_5 VLSI 2011	Hf/HfO_x IEDM 2011
switching type	unipolar	bipolar	unipolar	bipolar	bipolar	bipolar	bipolar	bipolar	bipolar	bipolar	bipolar
structure	1T-1R	1T-1R	1T-1R	1T-1R	1T-1R	1T-1R	1T-1R	1R	1T-1R	1R	1T-1R
cell area (μm^2)	~0.2	~0.03	~0.49	~0.25	~0.1	0.0009 (30nm)	0.0036 (60nm)	0.0025 (50nm)	~1	~9000	0.0001 (10nm)
speed	~5µs	~50ns	~5ns	~10ns	~5ns	~0.3ns	~50ns	~40ns	N/A	~10ns	~10ns
peak voltage	<3V	<3V	<3V	<2V	<1.5V	<2.5V	<3V	<2V	<2V	<2.5V	<1.5V
peak current	~2mA	~45µA	~100µA	~170µA	~25µA	~200µA	~1mA	~50µA	~50nA	~30µA	~50 µA
HRS/LRS ratio	>10	>10	>90	>10	>100	>100	>10	>10	>100	>100	>10
endurance	10^6	600	100	10^9	10^6	10^{10}	10^6	10^6	10^5	10^{12}	$5x10^7$
retention	300h@ 150℃	30h@ 90℃	1000h@ 150℃	3000h@ 150℃	10h@ 200℃	28h@ 150℃	2000h@ 150℃	28h@ 125℃	28h@ 125℃	3h@ 200℃	30h@ 250℃

Fig. 2. A Representative List of Binary Metal-Oxide RRAM device characteristics. Data Are Collected From [8], [40], [41], [42], [14], [36], [43], [44], [45], [46], and [38]

On scaling down the memory devices HRS resistance increases (somewhat following the Ohm's law). While the LRS resistance remains more or less independent of the cell area. This is because conduction current during the LRS is mainly due to the filamentary conduction current. Hence overall scaling down the size benefits us by increasing the resistance ratio of HRS/LRS.

To take care of the power consumption of the device we must ensure that the peak reset current is low. It is observed that reset current decreases very slightly on decreasing the size of the device, which in turn increases the current density required for reset. This problem can be alleviated by reducing the compliance current during the set process as they are fairly linearly related. However, one must note that with a decrease in compliance current, the LRS increases. Fortunately, since scaling down also increases the HRS, therefore, we can tolerate some increase in LRS to achieve lower reset current.

V. FUTURE OUTLOOK

In the last decade, the research in this field has intensified. Especially, the binary metal-oxides that uses materials of interest to the semiconductor industry, have drawn a lot of attention. This technology is envisioned as a non-volatile memory which is fast, scalable, and compatible to conventional CMOS technology. A few highlights of the research development in this area is mentioned in Fig. 2. Some of the interesting applications of metal-oxide RRAM include embedded systems, artificial synapse element, and reconfigurable logic. As rightly mentioned in [39], there is enormous opportunity to rethink the memory design and extract orders of magnitude improvement in terms of performance and power efficiency.

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