PHASE LOCKED LOOP

(Design and Implementation)

A Project Report

submitted by

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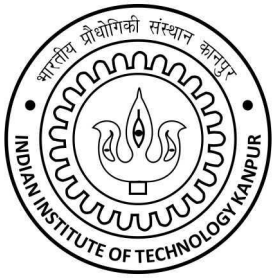
in partial fulfilment of the requirements
for the award of the degree of

BACHELOR OF TECHNOLOGY



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ABSTRACT

KEYWORDS: Phase Locked Loop (PLL) ; Phase Frequency Detector (PFD) ; Charge Pump (CP) ; Low Pass Filter (LPF) ; Current Starved Voltage Controlled Oscillator (CSVCO) ; Frequency Divider (FD)

This thesis presents a design for clock generating circuitry using PLL techniques. A simple design of CPPLL is followed by design of linear CSVCO. Feedback is provided through a *divide-by-2* frequency divider. The reference signal is 4 MHz square wave from a crystal oscillator and the technology used is 180 nm (SCL PDK). The design is optimised for low area and low power consumption.

CONTENTS

CHAPTER 1

INTRODUCTION

Concept of PLL was introduced in 1930s and since then the scope of PLL application has attracted many designers. With the advancement of the technology new designs, new problems and non idealities are emerging and hence the motivation to work in this field. PLL has vast application in the area of electronics and communication. PLL can be used for clock generation for a microprocessor, as a frequency synthesizer in a mobile, etc. In this thesis we would focus on the clock generation aspect of the PLL.

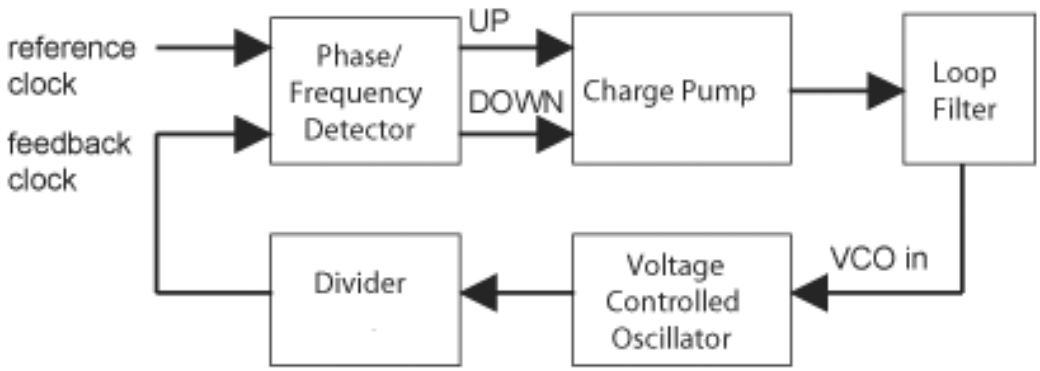

Figure 1.1: Block Diagram

The basic structure of the PLL can be understood from the block diagram above. The following chapters will explain each of these components, but the main focus will be on their design aspects.

CHAPTER 2

Phase Frequency Detector & Charge Pump

2.1 PFD

PLL is a feedback system that keeps the input signal aligned, w.r.t phase, to the reference signal. There are various implementations of PLL. Here we choose to implement Charge-Pump PLL as type I PLLs have tight trade-offs (between ω_{LPF} and ζ, the damping ratio) and have limited acquisition range. In order to remedy the acquisition problem, frequency comparison is also done in addition to the phase detection, as shown in Fig 2.1. For the periodic signals it is possible to merge both, frequency and phase, feedback loops and this role is played by Phase Frequency Detector.

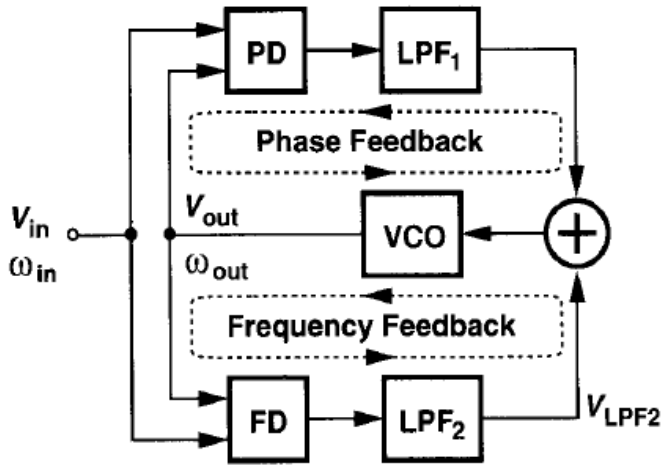

Figure 2.1: Aided Acquisition using Frequency Detection

The operation of PFD can be easily understood from Fig 2.2. Lets assume Q_a and Q_b are zero initially. Thus when input A rises (before input B), this results in Q_a being high but Q_b still low. The circuit will remain in this state until B rises, at which point Q_a will return to zero and Q_b will still be zero. Similar goes for Q_b and Q_a when input B rises before input A. It can be easily observed that in Fig 2.2 (a) Q_a represents the phase difference (ϕ_A - ϕ_B) between the inputs whereas in Fig 2.2 (b) Q_a represents the frequency variation (ω_A - ω_B) between the inputs.

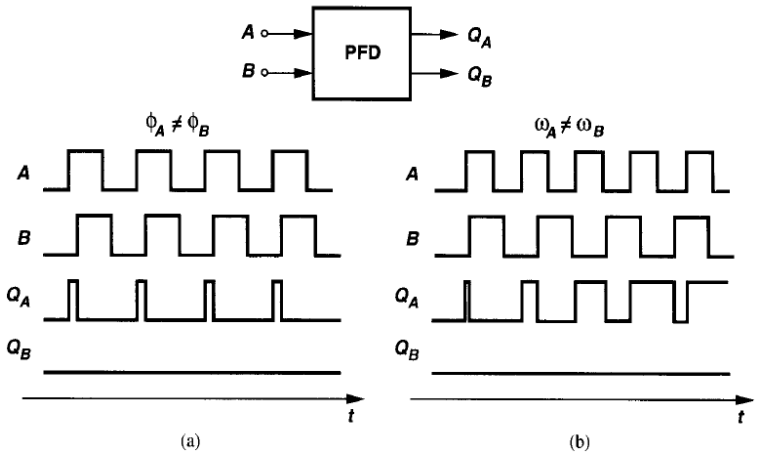

Figure 2.2: PFD Operation

PFD can be implemented as shown in Fig 2.3 i.e. two edge triggered resettable D flip flops with their D inputs tied to logic one.

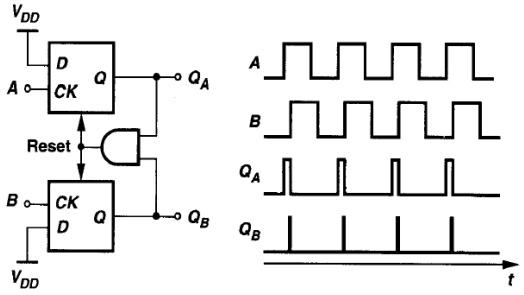

Figure 2.3: PFD Implementation

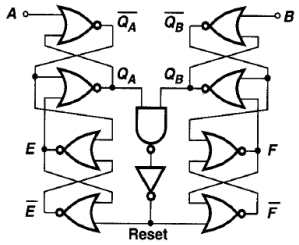

Figure 2.4: PFD at Gate Level

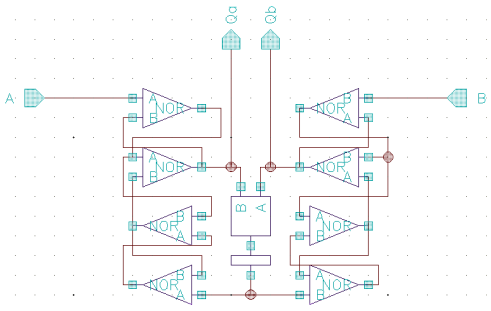

Figure 2.5: PFD Realisation

2.2 Charge Pump

Since the difference between the average values of Q_a and Q_b is of interest to us, therefore the outputs of Q_a and Q_b can be directly passed through a LPF and sensed differentially, as shown in Fig 2.6. However, a more conventional way is to introduce a Charge Pump between a PFD and LPF.

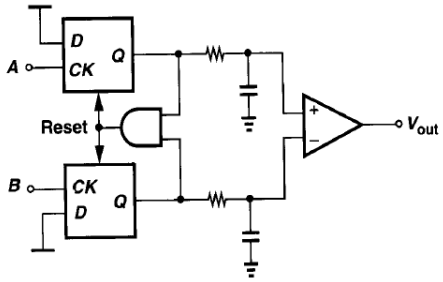

Figure 2.6: PFD followed by LPF

A charge pump consists of two switched current sources that may pump charge in or out of the loop filter according to the logic states of Q_a and Q_b. I_1 and I_2 are generally equal and referred as Up and Down currents respectively.

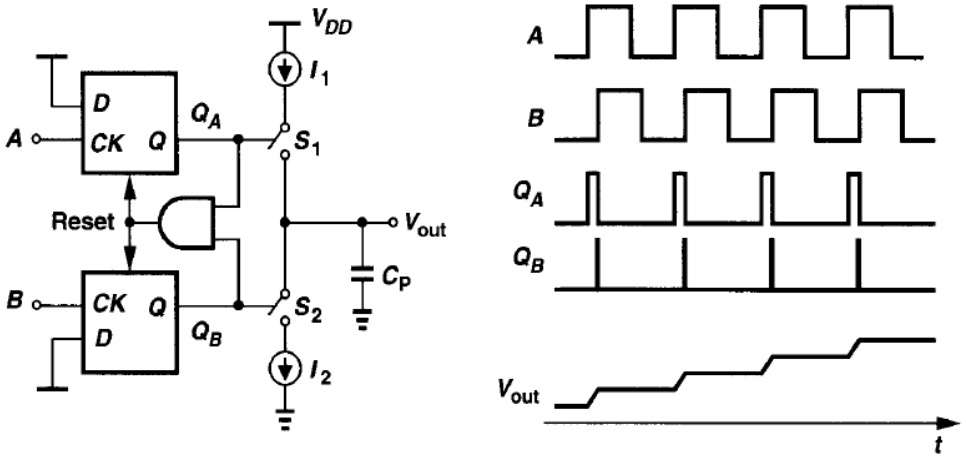

Figure 2.7: PFD along with Charge Pump

Charge pump can be easily implemented using MOSFETs as shown on the Fig 2.8 (a). Here $M1$ and $M2$ operates as current sources, and $M3$ and $M4$ operate as switches. An immediate drawback of this implementation can be seen as the inputs to the charge pump are reaching CP at different times, due to the delay caused by the inverter. This error can suppressed by inserting a transmission gate between Q_b and the gate of $M3$, equalizing the delays [Fig 2.8 (c)].

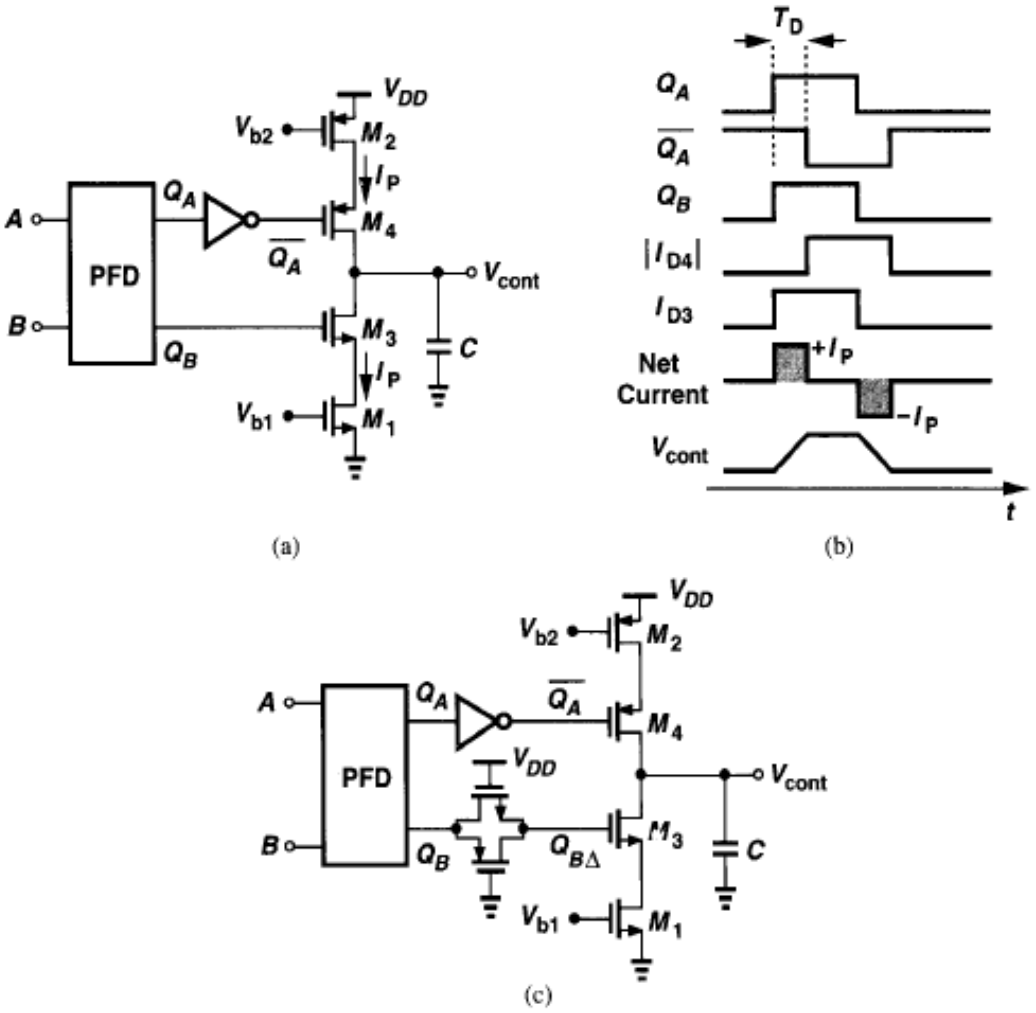

Figure 2.8: (a) Implementation of Charge Pump (b) Effect of skew between $\overline{Q}_a$ and Q_b (c) Suppression of skew by transmission gate

The design presented above can be further improved to tackle the problem of Bootstrapping. This problem originates due to finite capacitance seen at the drains of the current sources. Suppose, as illustrated in Fig 2.9, S_1 and S_2 are off. This allows C_X to discharge to ground and C_Y to charge to V_{DD}. In the next instant, when both S_1 and S_2 are on, $V_X \approx V_Y \approx V_{cont}$ (assuming the voltage drop across S_1 and S_2 to be zero). If the phase error is zero and $I_{D1} = I_{D2}$, even if $C_X = C_Y$, change in V_X and V_Y will not be same and would result in sudden jump of V_{cont}, which should remain constant ideally. Therefore this creates a problem. The design solution of this problem will not be discussed here.

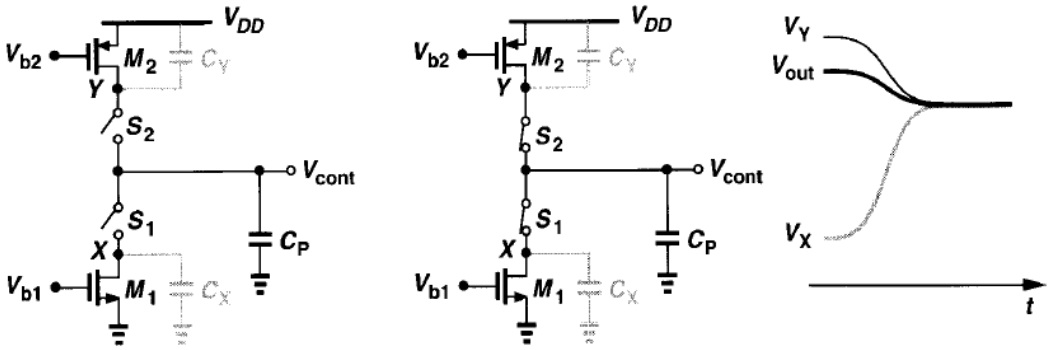

Figure 2.9: Bootstrapping

CHAPTER 3

Current Starved Voltage Controlled Oscillator & Frequency Divider

3.1 CSVCO

Introduction

An oscillator produces periodic output, generally in the form of voltage. Most applications require to control the output frequency of the oscillator. Here is where VCO comes into picture. VCO provides us the capability to control the frequency of the oscillator by tuning its input voltage i.e VCO is a voltage to frequency converter.

Design and Operation

VCO is designed according to the design parameters mentioned in Table 3.1.

Table 3.1: VCO Design Specifications

Power Supply (V_{DD})	1.8 V
Centre Frequency	8 MHz
Inverter Delay	2.18ns
Technology	180nm (SCL PDK)

There are several architectures for designing VCO. Here we choose to design and analyze Current Starved VCO. Current Starved architecture is preferred as it is less sensitive to the voltage variation in V_{DD}. The basic structure of VCO is designed using Ring Oscillator and further to implement the current starved architecture current mirrors are used.

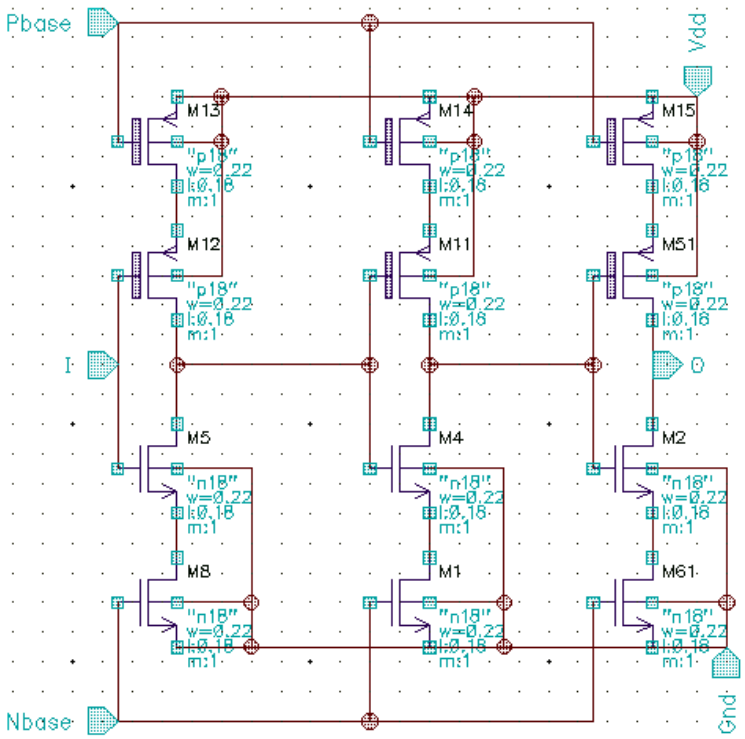

Figure 3.1: Building block of Ring Oscillator (with Current Mirrors)

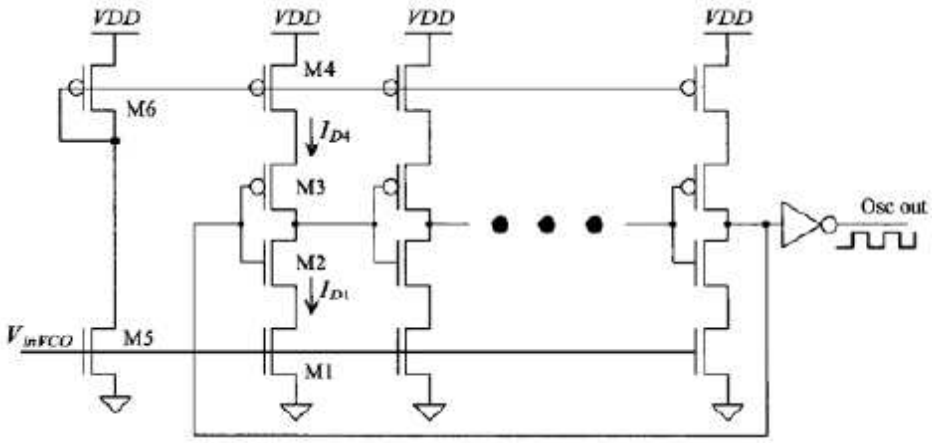

Figure 3.2: Schematic of CSVCO

The operation of CSVCO is similar to that of a ring oscillator. MOSFETs M2 and M3 operate as inverter while M1 and M4 operate as current sources, as illustrated in Fig 3.2. The current through M5 and M6 is mirrored into each inverter stage and is controlled by V_{inVCO}. Hence the inverter stages are starved for current.

Frequency of Oscillation

Total capacitance at the drains of M2 and M3 is given by

$$C_{tot} = C_{out} + C_{in} \tag{3.1}$$

$$C_{tot} = C'_{ox}(W_pL_p + W_nL_n) + \frac{3}{2}C'_{ox}(W_pL_p + W_nL_n) \tag{3.2}$$

$$C_{tot} = \frac{5}{2}C'_{ox}(W_pL_p + W_nL_n) \tag{3.3}$$

where C_{out} and C_{in} simply represent the input and output capacitances of the inverter. The time taken to charge C_{tot} for zero to V_{SP} (switching point of the inverter) with constant current I_{D4} is given by

$$t_1 = C_{tot}\frac{V_{SP}}{I_{D4}} \tag{3.4}$$

While the time taken to discharge C_{tot} from V_{DD} to V_{SP} is given by

$$t_2 = C_{tot}\frac{V_{DD} - V_{SP}}{I_{D1}} \tag{3.5}$$

Since I_{D1} = I_{D4} = I_D, therefore

$$t_1 + t_2 = \frac{C_{tot}.V_{DD}}{I_D} \tag{3.6}$$

Hence the oscillation frequency of a CSVCO with N (odd >3) number of inverter stages is

$$f_{osc} = \frac{1}{N(t_1 + t_2)} = \frac{I_D}{N.C_{tot}.V_{DD}} \tag{3.7}$$

Linearization

Many applications require VCO to be linear i.e. output frequency is linearly related to the input voltage. This can implemented in the following manner:

From Eq. (3.7) it can be observed that f_{osc} linearly varies w.r.t I_D. Therefore it is required that the current flowing through the MOSFETs varies linearly w.r.t the input voltage of VCO. This can be achieved by designing as shown in the Fig 3.3. The width of M5R is made wide so that its V_{GS} is always approximately V_{TN}. This ensures that

drain current is linearly proportional to V_{inVCO}.

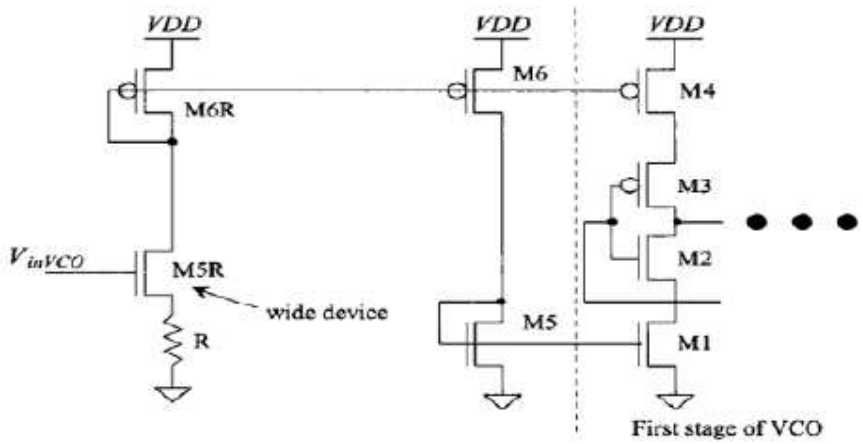

Figure 3.3: Linearizing VCO gain

Simulation and Results

Full schematic of the Current Starved VCO is shown in Fig 3.4. Fig 3.5 represents the linearity of the CSVCO.

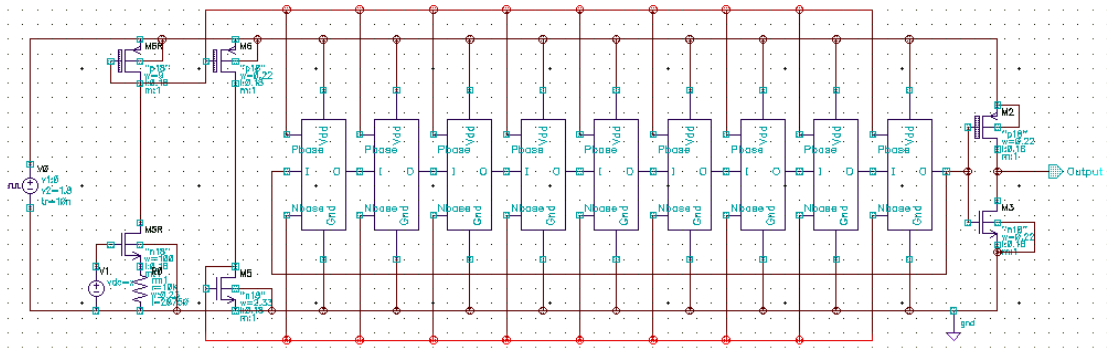

Figure 3.4: Current Starved VCO

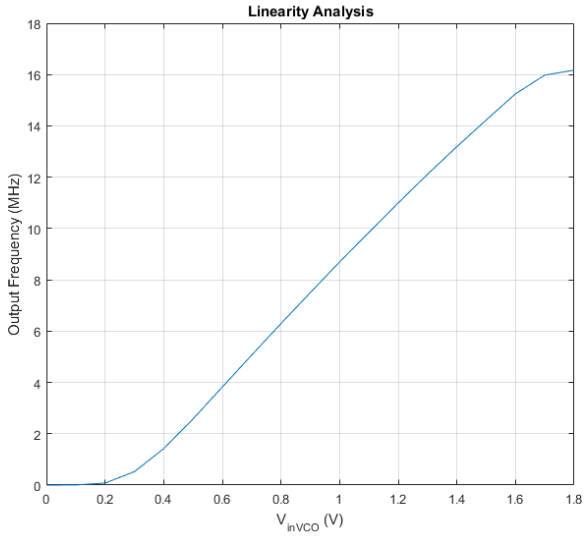

Figure 3.5: V_{inVCO} vs Output frequency

The CSVCO is designed and simulated using SCL PDK 180nm CMOS Technology. The voltage supply (V_{DD}) is taken to be 1.8V. The output frequency ranges from 0 MHz to 16.172 MHz, centred around 8 MHz, linearly w.r.t the input of VCO (V_{inVCO}). The maximum power consumption by CSVCO is 181.161μW.

3.2 Divide-by-2 Frequency Divider

Divide-by-2 frequency divider is used to provide feedback form CSVCO to PFD. It is simply implemented using D flip flops, as shown in the Fig 3.6. This structure reduces the time jitter of the VCO.

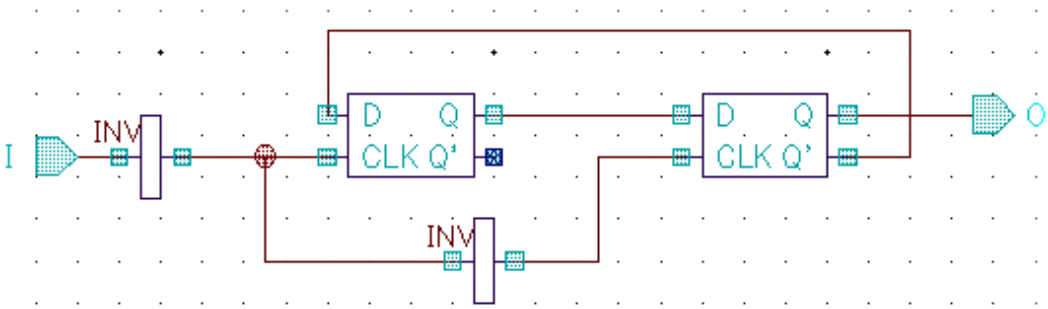

Figure 3.6: Divide-by-2 Frequency Divider

CHAPTER 4

Stability Analysis (LPF)

4.1 Transfer Function of VCO

Ideally VCO should be capable of transferring input voltage to output frequency linearly.

$$\omega_{out} = \omega_0 + K_{VCO}V_{cont} \tag{4.1}$$

Here, ω_0 represents the intercept corresponding to $V_{cont} = 0$ and K_{VCO} denotes the gain of the VCO (rad/s/V). The achievable range $\omega_2 - \omega_1$, is called tuning range of the VCO.

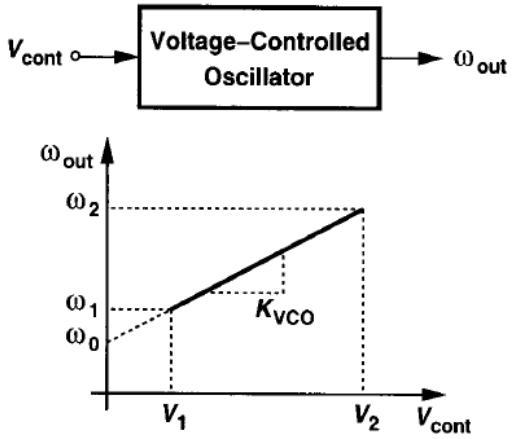

Figure 4.1: Ideal VCO transfer function

Due to the non ideal behaviour, the transfer function of VCO is modelled as

$$\frac{\phi_{out}}{V_{cont}} = \frac{K_{VCO}}{s} \tag{4.2}$$

4.2 Transfer Function of PFD/CP/LPF combination

The combination of PFD, CP and LPF (as shown in Fig 2.7) doesn't represent a linear system however we model their behaviour linearly assuming the ramp approximation,

as shown in Fig 4.2.

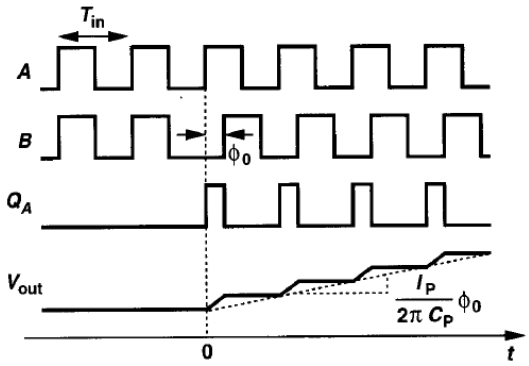

Figure 4.2: Step response of PFD/CP/LPF combination (ramp approximation)

Let us assume the period of the input is T_{in} and the charge pump provides the current of $\pm I_P$. As shown in the Fig 4.2, initial phase difference is zero and at $t = 0$ step phase of ϕ_0 is applied to input B i.e. $\Delta\phi = \phi_0 u(t)$. As a result Q_A continues to produce pulses of width $\phi_0 T_{in}/2\pi$. This resulted in raising of output voltage by (I_P/C_P) times the Q_A pulse width. Therefore

$$V_{out}(t) = \frac{I_P}{2\pi C_P} t.\phi_0 u(t) \tag{4.3}$$

Impulse response is therefore given by its derivative

$$h(t) = \frac{I_P}{2\pi C_P} u(t) \tag{4.4}$$

Hence the transfer function of the combination is given by

$$\frac{V_{out}}{\Delta\phi_0}(s) = \frac{I_P}{2\pi C_P}\frac{1}{s} \tag{4.5}$$

4.3 Stability Analysis

Now let us construct the linear model of the charge pump PLL. This would yield the open loop transfer function as

$$\frac{\phi_{out}}{\phi_{in}}(s) = \frac{I_P}{2\pi C_P}\frac{K_{VCO}}{s^2} \tag{4.6}$$

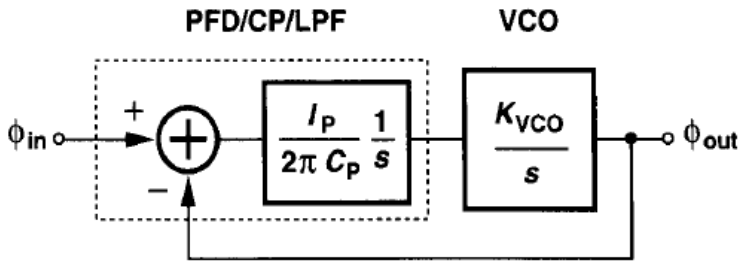

Figure 4.3: Linear model of CPPLL

It can be easily observed that the the closed loop response will have two imaginary poles which would result in instability of the system. Hence to stabilize the system it is suggested to add a resistor R_P in series with the capacitor C_P in the low pass filter. But since the charge pump drives the series combination of R_P and C_P, each time a current is injected in the loop filter, the control voltage experiences a large jump. Hence to minimize the ripple effect, a small capacitor C_2 ($\sim$ 0.2 - 0.1 times C_P) is added in parallel to their series combination.

Hence the final LPF is modified as shown in Fig 4.4 in order to attain and enhance stability.

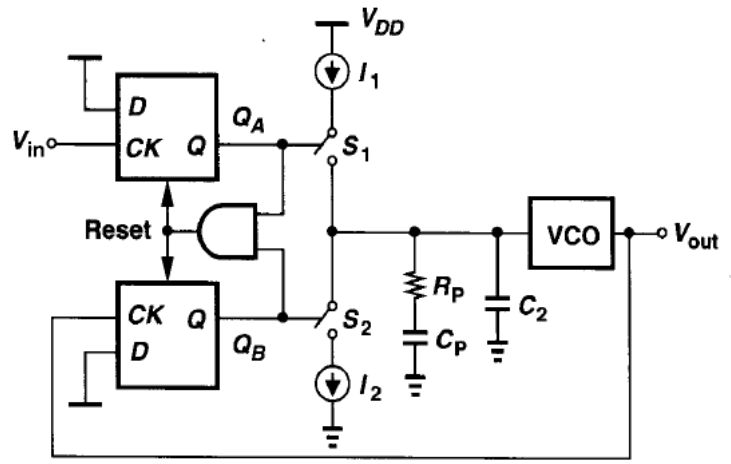

Figure 4.4: Improved LPF to attain stability and reduce ripple in V_{inVCO}

CHAPTER 5

RESULTS

The full schematic of the PLL is shown in Fig 5.1.

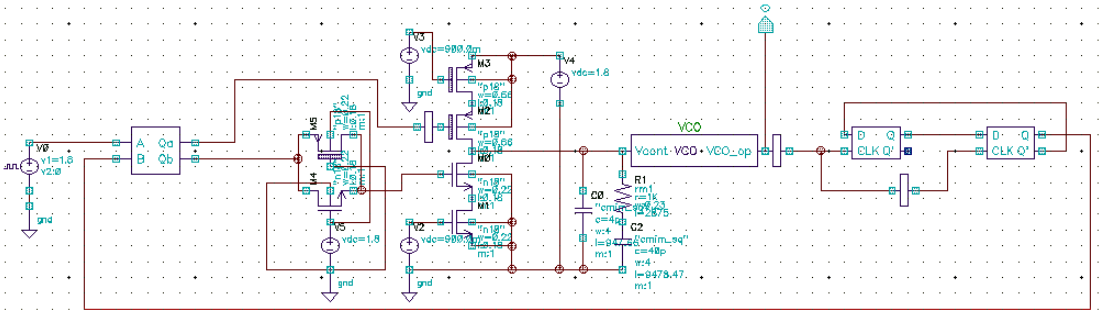

Figure 5.1: Complete PLL schematic

The PLL is working as expected and producing an output frequency of 8 MHz. Settling time of the PLL ($\pm 5\%$) is around 33μs and Lock time is around 125μs which is practical.

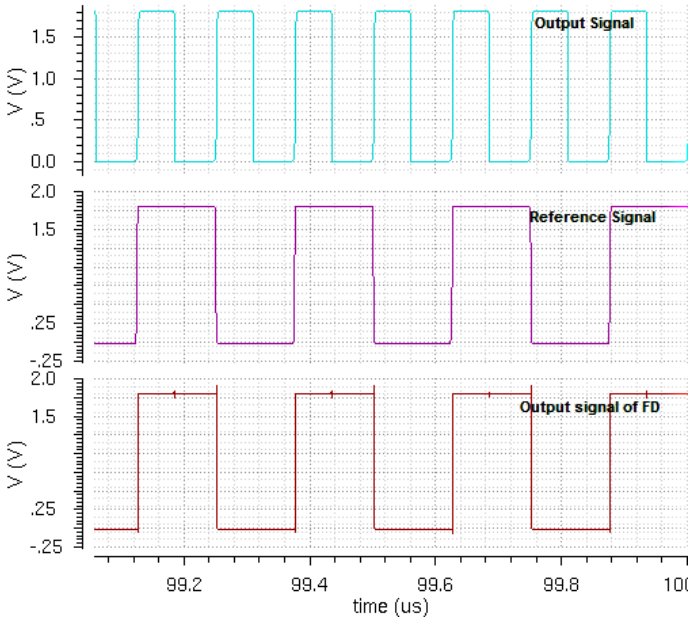

Figure 5.2: Waveforms observed from the PLL

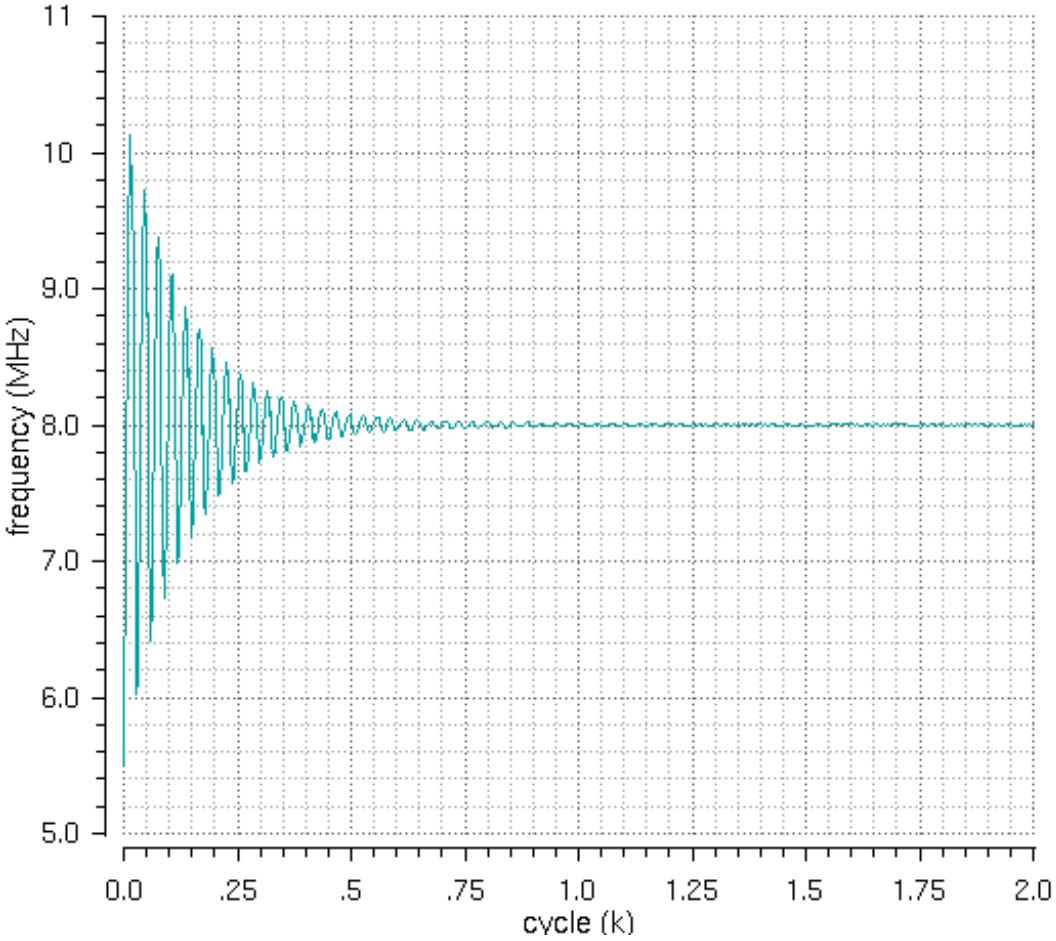

Figure 5.3: Output Frequency

CHAPTER 6

CONCLUSION

The PLL circuit is designed and simulated using SCL PDK 180nm CMOS Technology. The voltage supply (V_{DD}) is taken to be 1.8V. The output frequency of the CSVCO ranges from 0 MHz to 16.172 MHz, centred around 8 MHz, linearly w.r.t the input of VCO (V_{inVCO}). Maximum power consumption by CSVCO is 181.161μW. After performing stability analysis, the values of R_P, C_P and C_2, used in the LPF, are taken to be 1kΩ, 40pF and 4pF respectively. The PLL is stable and is producing an output frequency of 8 MHz. Settling time of the PLL ($\pm 5\%$) is around 33μs and Lock time is around 125μs.

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