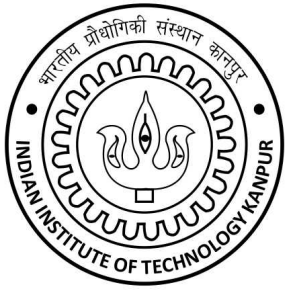
Indian Institute of Technology Kanpur



Phase Locked Loop (Design and Implementation)

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Candidate

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Motivation

- Concept of PLL was introduced in 1930s and since then the scope of PLL application has attracted many designers.
- With the advancement of the technology new designs, new problems and non idealities are emerging and hence the motivation to work in this field.
- PLL has vast application in the area of electronics and communication.
  - Clock generation for a microprocessor
  - Frequency synthesizer in a mobile
  - Skew reduction

Block Diagram of PLL

- The basic structure of the PLL can be understood from the block diagram below.

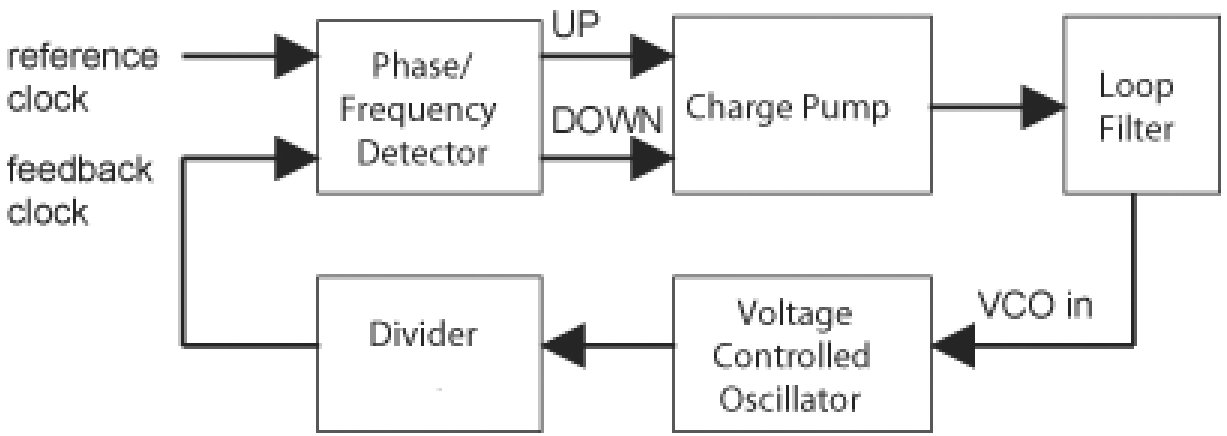

Figure: Block Diagram

Work Plan

- In the early pre-mid semester (January), through literature survey was conducted on VCO and its working.
- Later part of the pre-mid semester (February) was devoted to design and implementation of VCO and frequency divider.
- In the similar fashion, during early post-mid semester (March), through literature survey was conducted on PFD, Charge Pump & LPF, and their working.
- Later part of the post-mid semester (late March and April) was devoted to design and implementation of PFD, Charge Pump and LPF. All the components were combined and stability analysis was performed. The results were recorded and a report was developed.

Final schematic of the PLL

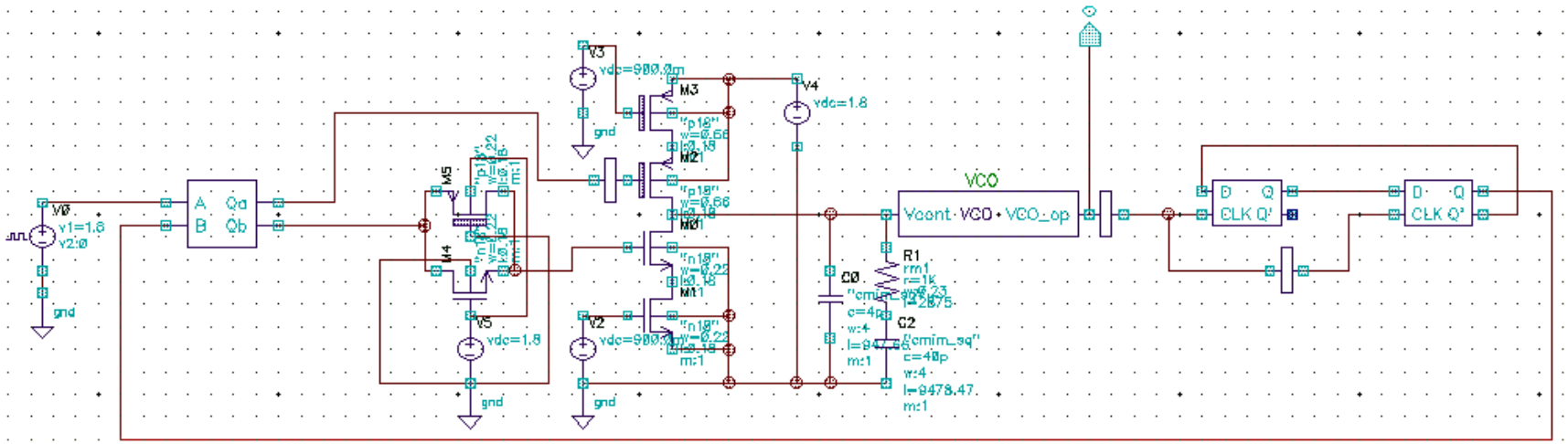

Figure: Complete PLL schematic

Results (VCO)

- The PLL circuit is designed and simulated using SCL PDK 180nm CMOS Technology. The voltage supply (V_{DD}) is taken to be 1.8V.
- The output frequency ranges from 0 MHz to 16.172 MHz, centred around 8 MHz, linearly w.r.t the input of VCO (V_{inVCO}).
- The maximum power consumption by CSVCO is 181.161μW.

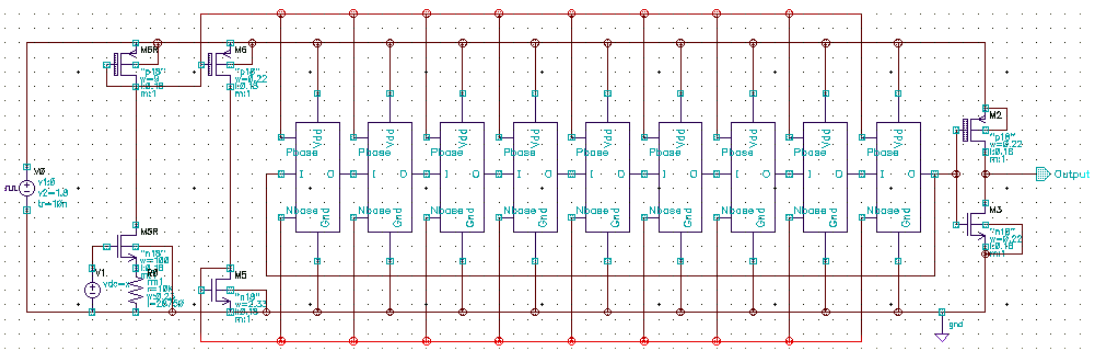

Figure: Current Starved VCO

Results (VCO and LPF)

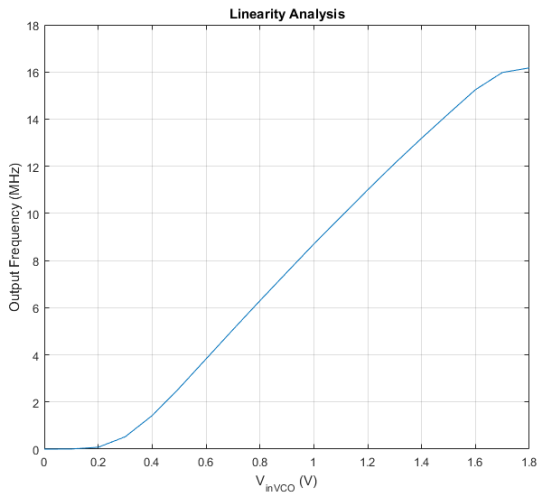

Figure: V_{inVCO} vs Output frequency

- After performing stability analysis, the values of R_P, C_P and C_2, used in the LPF, are taken to be 1kΩ, 40pF and 4pF respectively.

Results (LPF)

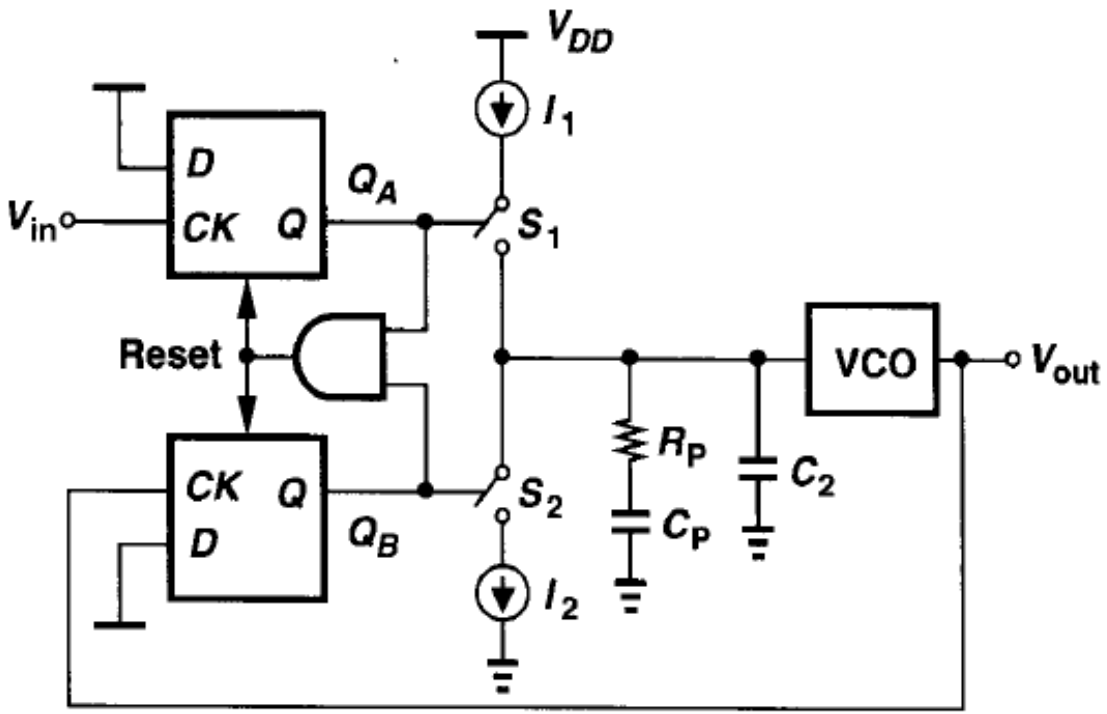

Figure: Improved LPF to attain stability and reduce ripple in V_{inVCO}

Results (PLL)

- The PLL is working as expected and producing an output frequency of 8 MHz.
- Settling time of the PLL ($\pm 5\%$) is around 33μs and Lock time is around 125μs which is practical.

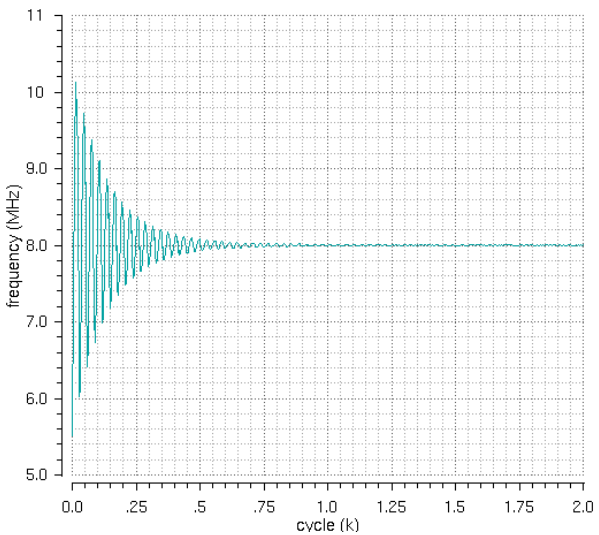

Figure: Output Frequency

Discussion

- Out of several architectures for designing VCO, I chose to design and analyze Current Starved VCO as it is less sensitive to the voltage variation in V_{DD}.
- Many applications require VCO to be linear i.e. output frequency is linearly related to the input voltage. Hence linearity is an important performance parameter for a VCO.
- Divide-by-2 frequency divider is used to provide feedback from CSVCO to PFD. This simple structure, using D flip flops, reduces the time jitter of the VCO.

Discussion

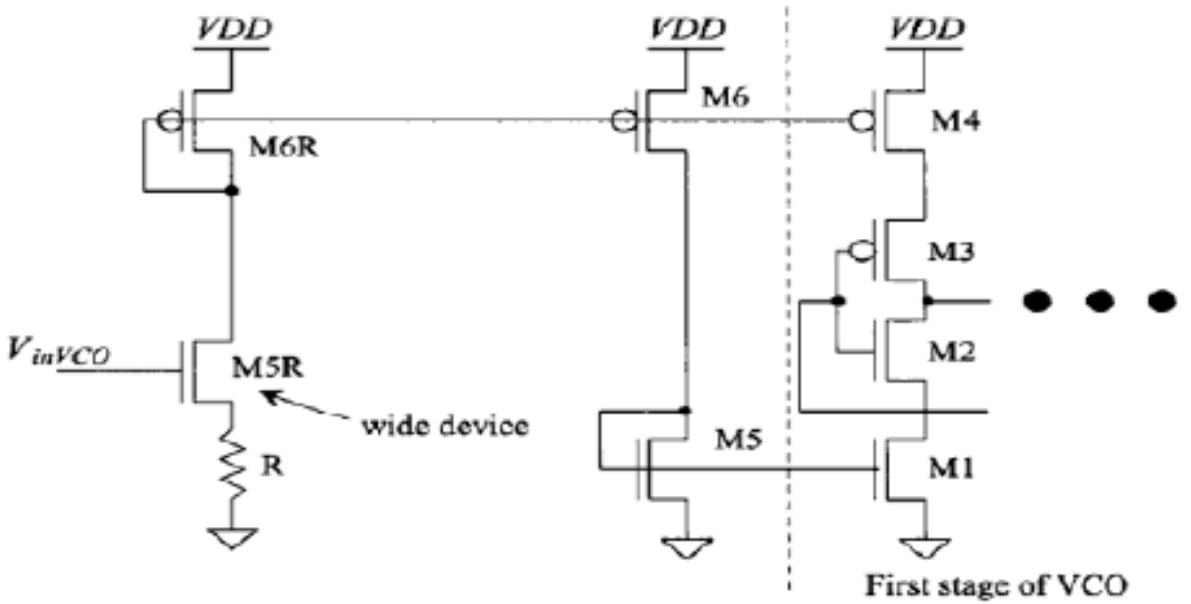

Figure: Linearizing VCO gain

Discussion

- There are various implementations of PLL. Here I chose to implement Charge-Pump PLL as type I PLLs have tight trade-offs and have limited acquisition range.
- Aided acquisition range is possible due to addition of frequency detector to the phase detector, using PFD.
- To remove the delay between the two inputs of the charge pump, a transmission gate is added between Q_B and the gate of MOSFET corresponding to S_2.
- After performing stability analysis it was observed that in order to minimize the ripple effect, a small capacitor C_2 ($\sim$ 0.2 - 0.1 times C_P) must be added in parallel to the series combination of R_P and C_P.

Discussion

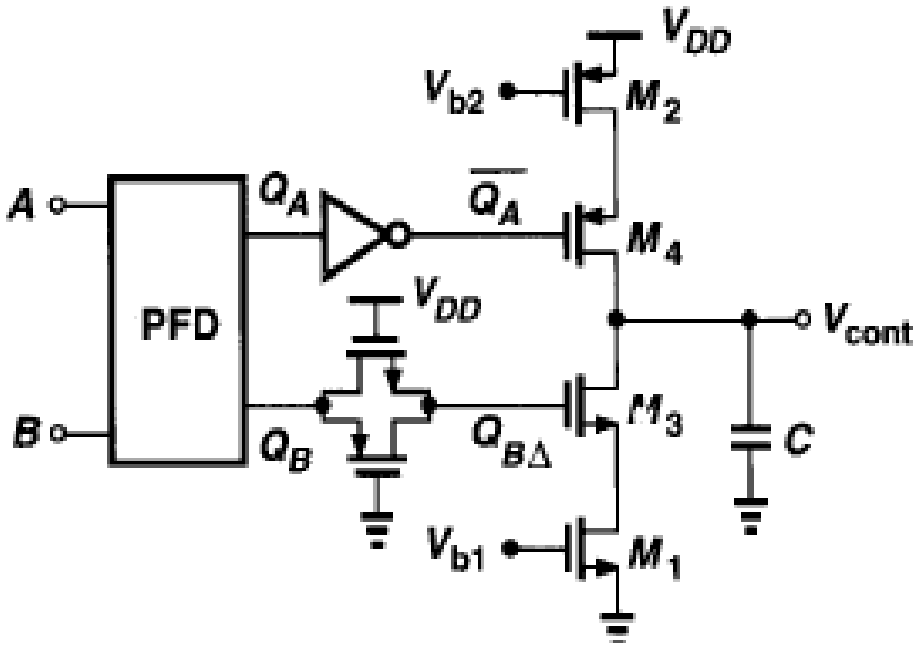

Figure: Suppression of skew by transmission gate

Summary of Results

- The PLL circuit is designed and simulated using SCL PDK 180nm CMOS Technology and the voltage supply (V_{DD}) is taken to be 1.8V.
- The output frequency of the CSVCO ranges from 0 MHz to 16.172 MHz, centred around 8 MHz, linearly w.r.t the input of VCO (V_{inVCO}).
- Maximum power consumption by CSVCO is 181.161μW.
- The PLL is stable and is producing an output frequency of 8 MHz.
- Settling time of the PLL ($\pm$5%) is around 33μs
- Lock time of the PLL is around 125μs.

Acknowledgements

My sincere thanks to Prof. S. Qureshi for mentoring me and making sure that I achieved practical results. He helped me learn focusing on the core ideas, and completely understanding the results. I would also like to thank Prof. S.S.K. Iyer and Prof. B. Mazhari, who came to my talk, asked crucial questions, and gave advice on further improvements of the design.